# Digital Electronic
# Third Grade

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# Digital Electronic

## Objectives of the Chapter

+ Explain how diodes and transistors can be used as electronic switches
+ Demonstrate an understanding of TTL devices, their parameters, how to drive them, and how to use them to drive external loads
+ Be familiar with CMOS-devices and characteristics
+ Understand TTL-to-CMOS and CMOS-to-TTL interfacing

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## 1.1 SWITCHING CIRCUITS

- The semiconductor devices used in digital integrated circuits (I Cs) include diodes, bipolar junction transistors (BJTI) and metal-oxide-semiconductor field-effect transistors (MOSFETs). The most popular transistor transistor logic (TTL) in use includes the 7400 and the 74LSOO families; resistors, diodes, and BJTs are the elements used to construct these circuits. The 74COO and the 74HCOO are the most widely used families constructed using MOSFETs. These two families of circuits are referred to as CMOS, since they use two different types of MOSFETs.. Virtually all digital ICs in use today are silicon, so let's see how a silicon diode or transistor is used as an electronic switch.

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**The Semiconductor Diode**

The symbol for a semiconductor diode (sometimes called a pn junction) is shown in Fig. 1.la. The diode behaves like a one-way switch. That is, it will allow an electric current in one direction but not the other. We will use conventional current flow rather than electron .flow. Figure 1.1 b shows the direction of current through a diode-this is the forward direction. When conducting current, a silicon (Si) diode will have a nominal voltage of 0. 7 V across its terminals as shown in Fig. 1.1 b. In this condition, the diode is said to be forward-biased. Notice that the triangle in the diode symbol points in the direction of forward current an easy memory crutch! It is not possible to pass current through the diode in the other direction-the reverse direction. When reverse-biased, the diode will act as an open switch as illustrated in Fig. 1.lc. To summarize:

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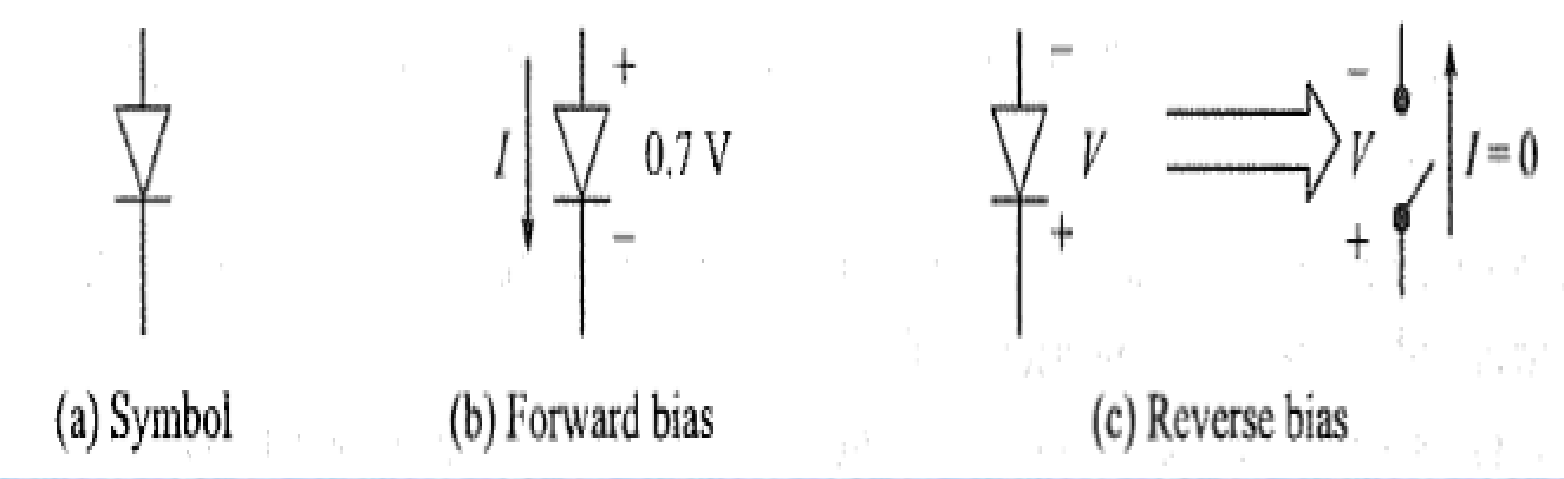


Figure 1.1 Semiconductor diode

1. When forward-biased, the diode conducts current, and the voltage across the diode terminals is about 0.7 Vdc.
2. When reverse-biased, the diode will not conduct current. The voltage across the diode terminals depends on the external circuit..

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- **Example 1.1**

**For each diode in Fig. 1.2, determine whether the diode is forward- or reverse-biased. Determine the diode current I in each case**

*Solution*

(a) The current direction is from +5 Vdc to ground, and thus the diode is forward-biased. The voltage across the diode terminals is 0.7 Vdc, and the diode current is found as

$$I = (5 - 0.7)/1\ \text{k}\Omega = 4.3/1\ \text{k}\Omega = 4.3\ \text{mA}$$

(b) The current direction is from +12 Vdc to ground, thus the diode is reverse-biased. The diode current is then $I = 0.0$ mA. There is no voltage across the 10-kΩ resistor, and thus the voltage across the diode terminals is 12 Vdc.

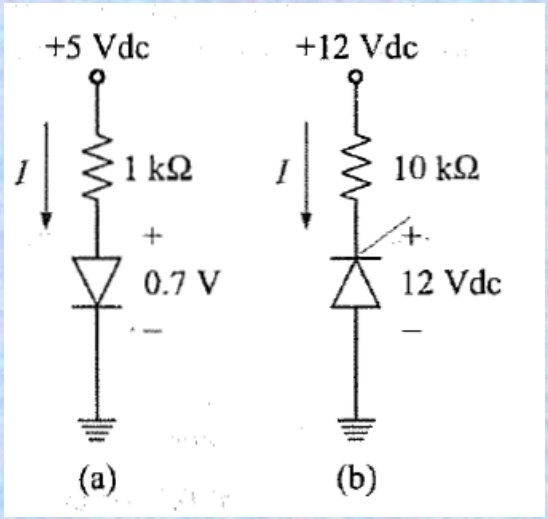


Figure 1.2

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**LEDs**

- The symbol for a light-emitting diode (LED) is shown in Fig. 1.3a. The arrows indicate light emission capability. The operation of an LED is similar to that of an ordinary diode. When forward-biased, it emits light in the visible spectrum and is thus used as an indicator. However, the voltage across the diode terminals when forward-biased($V_f$) is somewhat greater than 0.7 Vdc. Typical LED forward voltages given in Fig. 1.3b shows that $V_f$ varies with the color of the emitted light. The color of the emitted light depends on the elements added to the semiconductor material during manufacturing.

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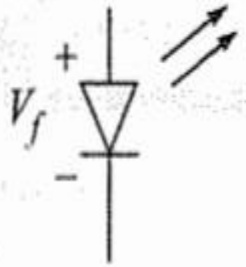


(a) Symbol

| | Red | Yellow | Green |
|---|---|---|---|
| $V_f$(V) | 1.6 | 2.2 | 2.4 |

(b) Typical forward voltages

Figure 1.3

**Example 1.2**

The diode in Fig. 1.2a is replaced with a red LED. What is the diode current?

**Solution** The diode is forward-biased, and the voltage across its terminals is about l.6 Vdc (Fig. 1.3b). The diode current is then

I = (5 - l.6)/1 kΩ = 3.4/1 kΩ = 3.4 mA

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**BJTs**

- The bipolar junction transistor (BJT) is available in two polarities (npn and pnp), as shown by the symbols in Fig. 1.4a. The BJT termninals are named collector, emitter, and base, as indicated. In Fig. 1.4b the BJT behaves as an electronic switch. The switch is activated by applying a voltage between base and emitter. Here's how it works:

1. The voltage between base and emitter is zero. The switch is open, and no current is allowed between collector and emitter. The transistor is off.
2. A voltage is applied between base and emitter. The switch is closed and a current is allowed between collector and emitter. The transistor is on. The voltage between emitter and collector (across a closed switch) is zero!

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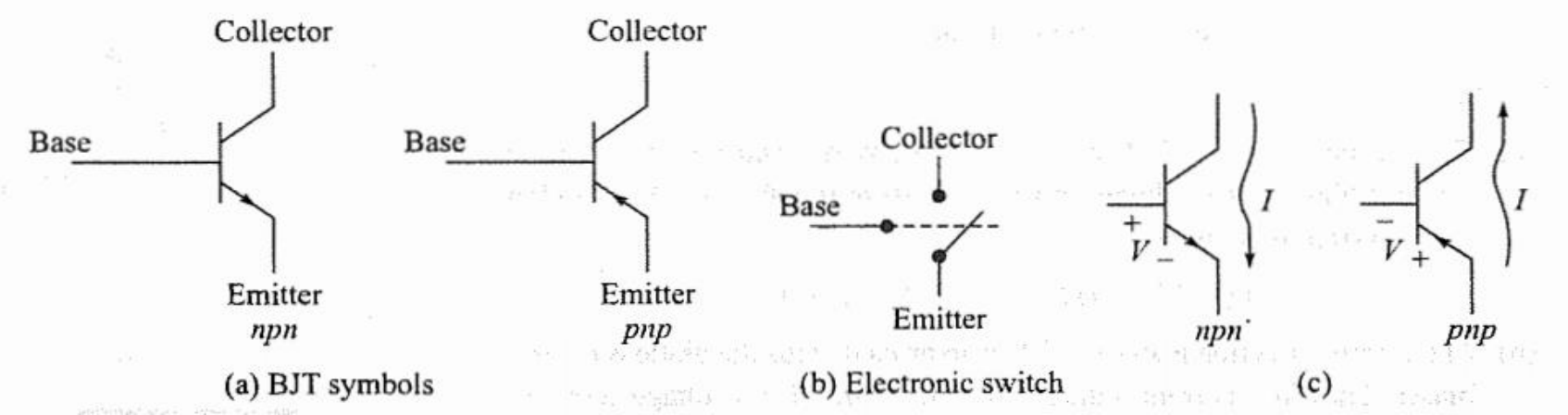


Figure 1.4

Since the BJT is available in two polarities-npn and pnp-the polarity of the applied base-emitter voltage must be as shown in Fig. 1.4c. For the npn, the **base** must be **more positive** than the **emitter**. The opposite is true for the pnp. This **base-emitter** voltage is applied across a forward-biased pn junction (a diode) and is thus limited to about 0. 7 Vdc. Care must be taken not to exceed 0. 7 Vdc, or the BJT may be destroyed.

The current through the npn transistor must be from collector to emitter as shown in Fig. 1.4c. For the pnp, current must be from emitter to collector. Notice that the current is in the direction of the arrow on the emitter-a good memory crutch! These polarities and current directions are important-you should make every effort to commit them to memory!

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**Example 1.3**

a. Determine the current $I$ and the voltage $V_2$ for the circuit in Fig. 1.5a if (i) $V_1 = 0$ Vdc, and (ii) $V_1 = +5$ Vdc.

b. Repeat part (a) for the circuit in Fig. 1.5b.

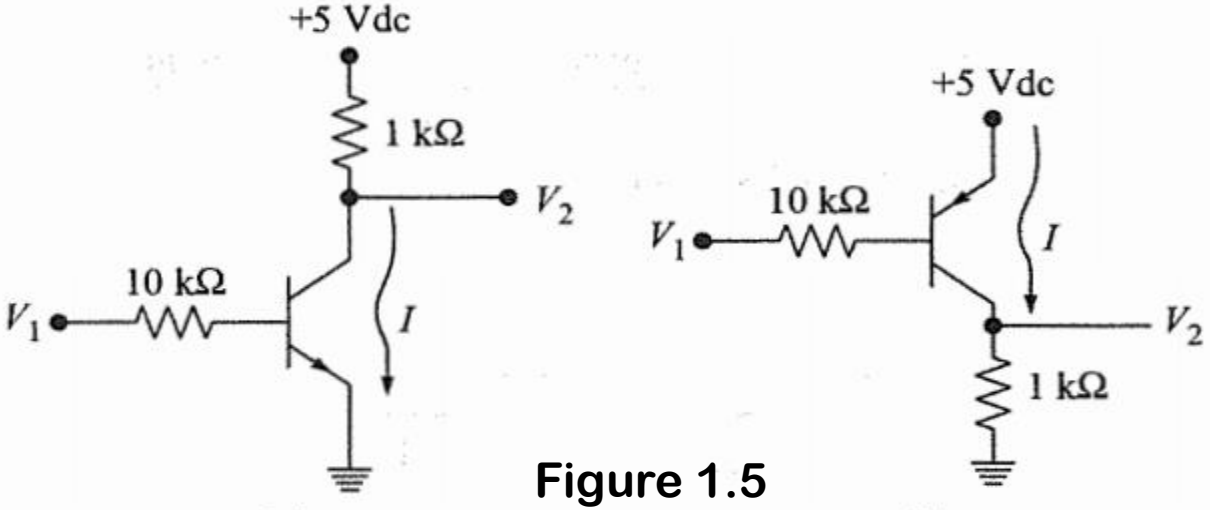


Figure 1.5

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**Solution**

a. $V_1$ =0 Vdc. There is no current in the 10 kΩ resistor. Thus the voltage base-emitter is zero. The BJT is off (switch is open). The BJT current and the current in the 1-kΩ resistor is zero. The voltage $V_2$ is +5 Vdc.

$V_1$=+5Vdc. The base is more positive than the emitter---- the BJT is on (switch is closed). $V_2$ is zero. The BJT current is *I*=5mA.

b. $V_1$ =0 Vdc. The base is more negative than the emitter--- the BJT is on (switch closed). $V_2$ is +5 Vdc. The BJT current is *I*=5mA.

$V_1$=+5Vdc. There is no current in the 10 kΩ resistor. The base is at +5Vdc, and so is emitter. Thus the voltage base-emitter is zero, and the BJT is off (switch open). The current *I*=0 mA, and $V_2$= 0 Vdc.

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Let's look carefully at the results from Example 1.3. For both circuits, when $V_1$ = 0 Vdc, $V_2$ = +5 Vdc. Also, when $V_1$ = +5 Vdc, $V_2$ = 0 Vdc. Clearly $V_2$ is always the **inverse** of $V_1$-in other words, each circuit in Fig. 1.5 is an inverter! Either of these circuits can be used to implement the basic inverter.

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MOSFETs

MOSFETs are available in two polarities (n-channel and p-channel) as shown by the symbols in Fig. 1.6a. MOSFETs operate as "depletion" or "enhancement" mode devices; the transistors in Fig. 1.6 are enhancement types. The MOSFET terminals are named gate, source, drain, and body as indicated. When the body is connected to the source, as is often the case with ICs, the simplified symbols are used. The MOSFET also behaves as the electronic switch in Fig. 1.6b. The switch is activated by applying a voltage between gate and source. Here's how it works:

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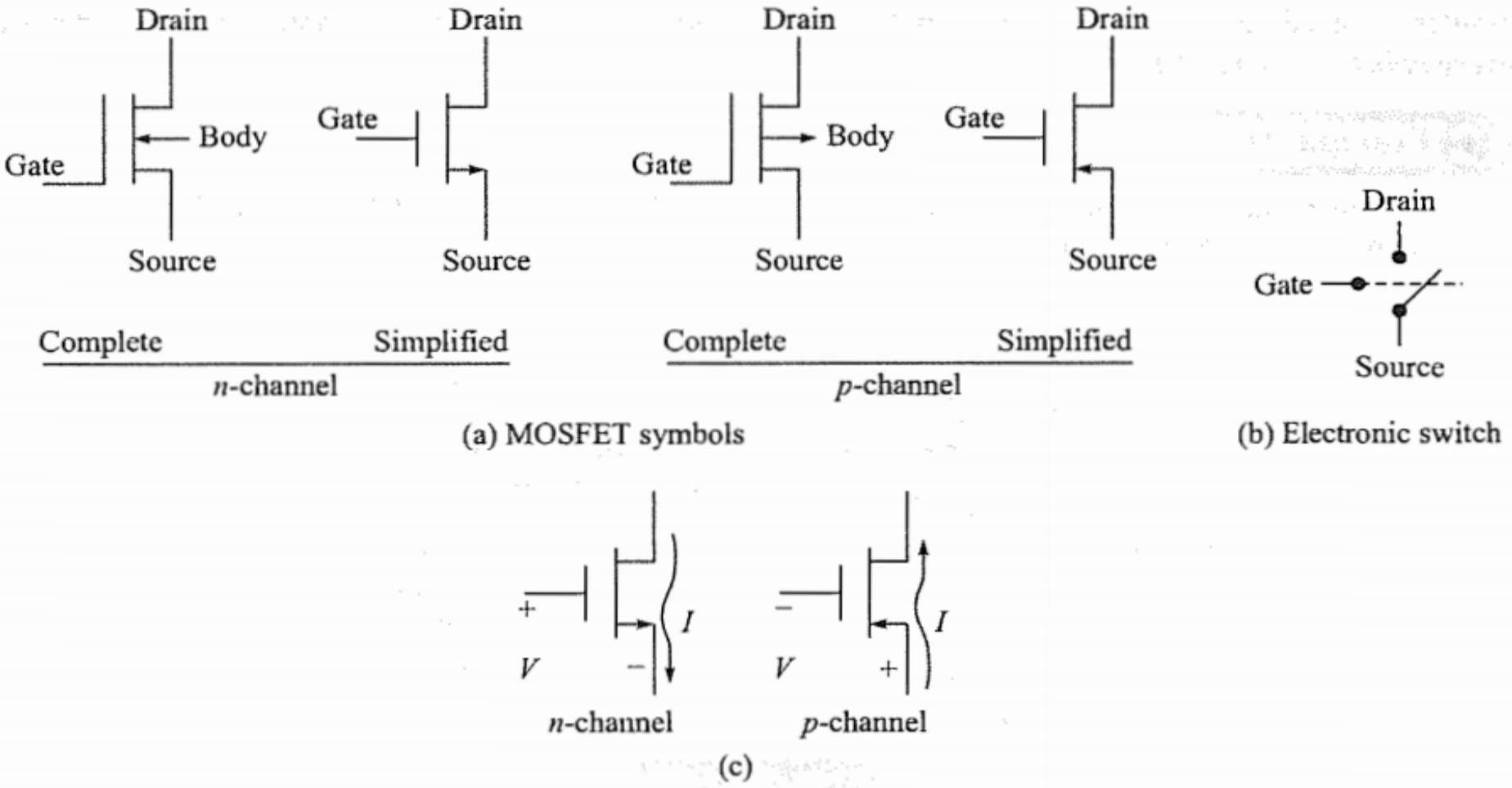


Fig. 1.6

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1. The voltage between gate and source is zero. The switch is open, and no current is allowed between source and drain. The transistor is off.
2. A voltage is applied between gate and source. The switch is closed, and a current is allowed between source and drain. The transistor is on. The voltage between source and drain (across a closed switch) is zero!

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- Since the MOSFET is available in two polarities-n-channel and p-channel-the polarity of the applied gate-source voltage must be as shown in Fig. 1.6c. For the n-channel transistor, the gate must be more positive than the source. The opposite is true for the p-channel transistor. The current through the n-channel transistor must be from drain to source as shown in Fig. 1.6c. For the p-channel transistor, current must be from source to drain. Notice that the current is in the direction of the small arrow on the drain-a good memory crutch! These polarities and current directions are important-you should make every, effort to commit them to memory!

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**Example 1.4**

An n-channel MOSFET can be used to construct a simple inverter as shown in Fig. 1.7. Determine the current $I$ and the output voltage $V_2$ if (a) $V_1 = 0$ Vdc, and (b) $V_1 = +5$ Vdc.

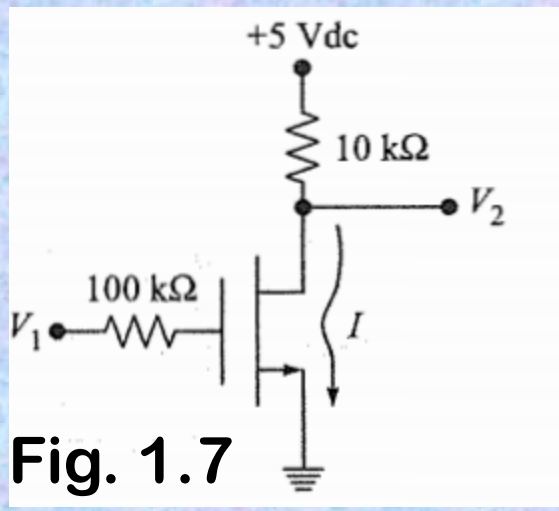


Fig. 1.7

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**Solution**

(a) $V_1$= 0 Vdc. There is no current in the 100-kΩ resistor, Thus the gate-source voltage is zero. The MOSFET is **off** (the switch is open). The MOSFET current and the current in the 10-kΩ resistor are zero. The voltage $V_2$ is +5 Vdc.

(b) $V_1$= +5 Vdc, The gate is_ more positive than, the source---the MQSFET is **on** (the switch is closed). $V_2$ is zero. The MOSFET current is /=.0.5 mA.

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- The small size of a MOSFET on an IC is one of the great advantages of ICs constructed using MOSFETs. The 10-KΩ resistor in Fig. 1.7 requires a large area on an IC compared to a MOSFET. A second MOSFET can be used in place of this resistor, as shown in Fig. 1.8. In this case, transistor $Q_1$ has its gate connected directly to its drain. When it is connected in this fashion, its behavior is similar to a resistor but shows little non-linearity compared to passive load, $Q_1$ is called an active load, and this circuit is a simple inverter.

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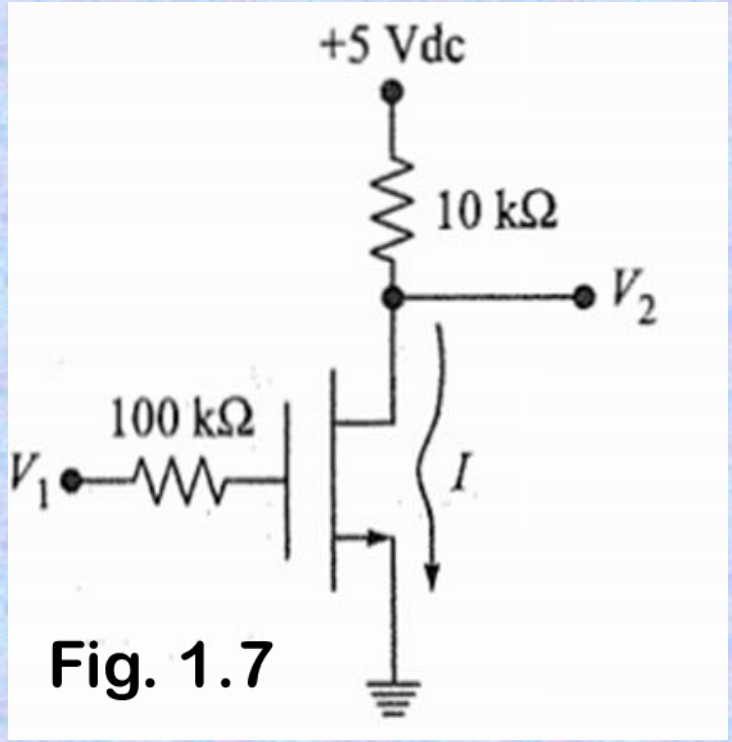


Fig. 1.7

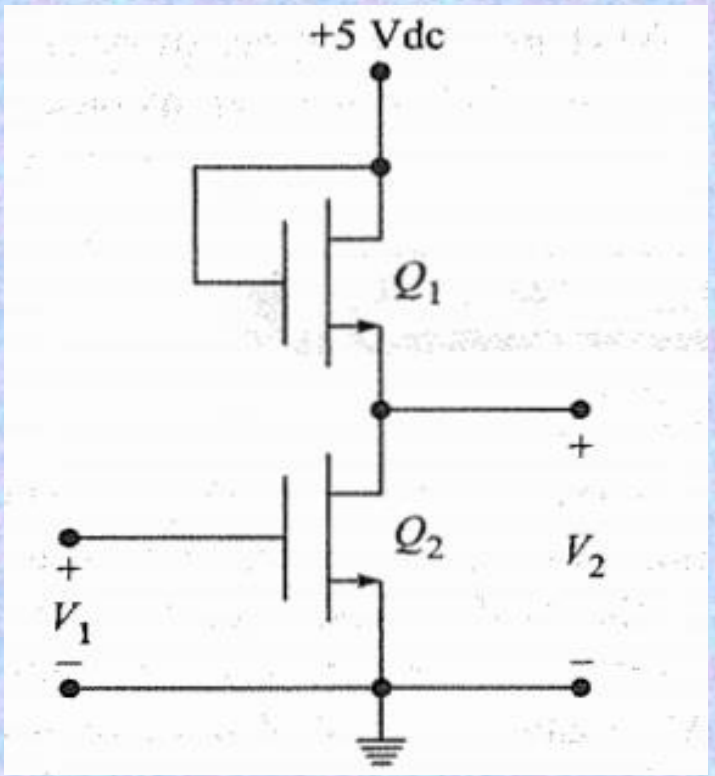


Fig.1.8

An inverter with active load

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## Complementary Metal-Oxide-Semiconductor (CMOS) FETs

- ICs constructed entirely with n-channel MOSFETs are called *NMOS* ICs. ICs constructed entirely with p-channel MOSFETs are called *PMOS* ICs. The 74C00 and 74HC00 families are constructed using both n-channel and p-channel MOSFETs. Since n-channel and p-channel MOSFETs are considered complementary devices, these ICs are referred to as ***CMOS*** ICs.

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- A CMOS inverter is shown in Fig. 1.9. Ideally, the characteristics of then channel are closely matched with the p channel. This circuit is the basis for the 74C00 and 74HC00 families. Here's how it works:

1. $V_1$= 0 Vdc. $Q_n$ is off and $Q_p$ is on. $V_2$ = +5 Vdc.
2. $V_1$= +5 Vdc. $Q_n$ is on and $Q_P$ is off. $V_2$ = 0 Vdc.

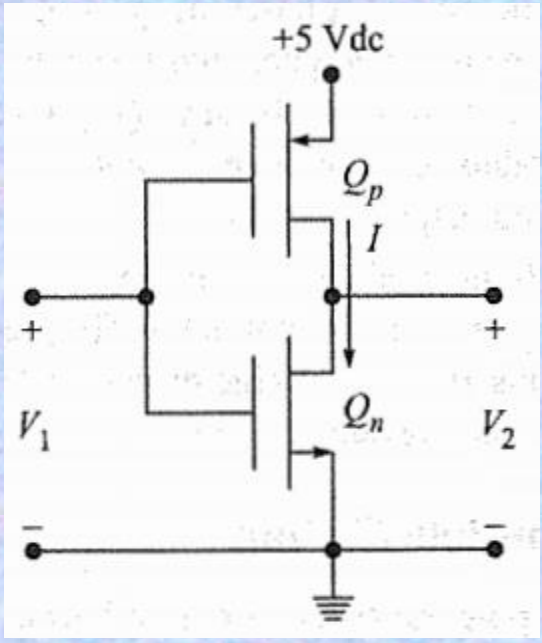


Fig 1.9. A CMOS inverter

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- Note that in the steady state (while not switching), one of the transistors is always ***off***. As a result, the current /= 0 mA. When switching between states, both transistors are **on** for a very short time because of the rise or fall time of $V_1$. This is the only time the current I is nonzero. This is the reason CMOS is used in applications where de power supply current must be held to a minimum-watches, pocket calculators, etc. **A word of warning**: If the input $V_1$ is held at +5 Vdc/2 = 2.5 Vdc, **both** transistors will be ***on***. This is an almost direct short between +5 Vdc and ground, and it won't be long before **both transistors expire**! So **don't impose this condition** on a CMOS IC.

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## 1.2 7400 TTL

Standard TTL

- Figure 1.10 shows a TTL NAND gate. The multiple-emitter input transistor is typical of the gates and other devices in the 7400 series. Each emitter acts like a diode; therefore, $Q_1$ and the 4-k$\Omega$ resistor act like a 2-input AND gate. The rest of the circuit inverts the signal so that the overall circuit acts like a 2-input NAND gate. The output transistors ($Q_3$ and $Q_4$) form a *totem-pole* connection (one npn in series with another); this kind of output stage is typical of most TTL devices. With a totem-pole output stage, either the upper or lower transistor is on. When $Q_3$ is on, the output is high; when $Q_4$ is on, the output is low.

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The input voltages A and B are either low (ideally grounded) or high (ideally +5 V). If A or B is low, the base of $Q_1$ is pulled down to approximately 0.7 V. This reduces the base voltage of $Q_2$ to almost zero. Therefore, $Q_2$ cuts off. With $Q_2$ open, $Q_4$ is off, and the $Q_3$ base is pulled high. The emitter of $Q_3$ is only 0.7 V below the base, and thus the Y output is pulled up to a high voltage.

On the other hand, when A and B are both high voltages, the emitter diodes of $Q_1$ stop conducting, and the collector diode goes into forward conduction. This forces $Q_2$ to turn on. In turn, $Q_4$ goes on and $Q_3$ turns off, producing a low output. Table 1.1 summarizes all input and output conditions.

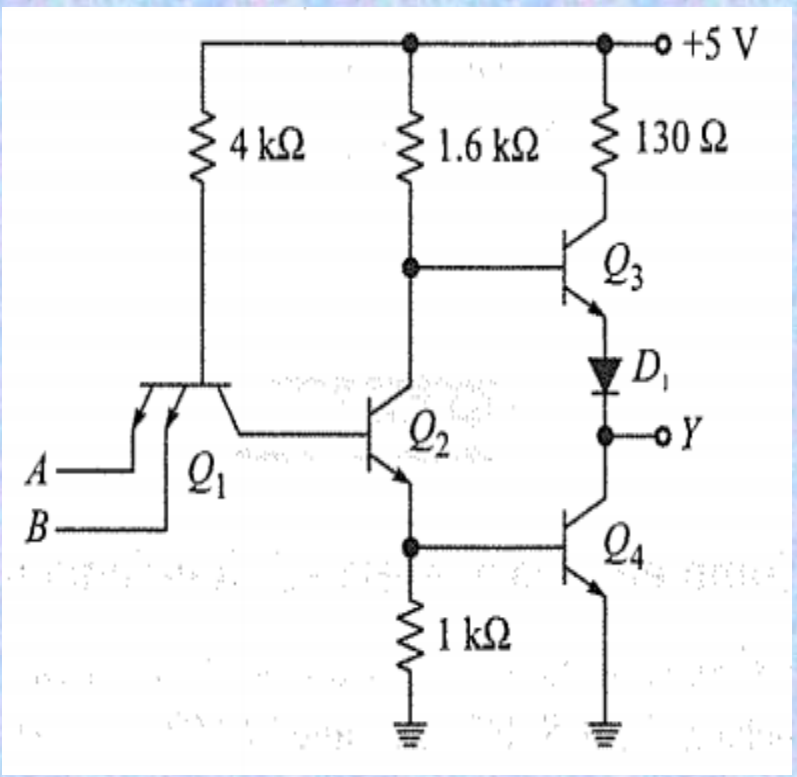


Fig. 1.10 Two-input TTL NAND gate

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Without diode $D_1$ in the circuit, $Q_3$ will conduct slightly when the output is low. To prevent this, the diode is inserted; its voltage drop keeps the base-emitter diode of $Q_3$ reverse-biased. In this way, only $Q_4$ conducts when the output is low.

| *A* | *B* | *C* |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Table 1.1 Two-Input NAND Gate

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**Totem-Pole Output**

- Totem-pole transistors are used because they produce a low output impedance. Either $Q_3$ acts as an emitter follower (high output), or $Q_4$ is on (low output). When $Q_3$ is conducting, the output impedance is approximately 70 ohms ($\Omega$); when $Q_4$ is on, the output impedance is only 12 $\Omega$ (this can be calculated from information on the data sheet). Either way, the output impedance is low. This means the output voltage can change quickly from one state to the other because any stray output capacitance is rapidly charged or discharged through the low output impedance.

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## Propagation Delay Time and Power Dissipation

- Two quantities needed for later discussion are power dissipation and propagation delay time. A standard TTL gate has a power dissipation of about 10 milliwatts (mW). It may vary from this value because of signal levels, tolerances, etc. but on the average it is 10 mW per gate. The propagation delay time is the time it takes for the output of a gate to change after the inputs have changed. The propagation delay time of a TTL gate is approximately 10 nanoseconds (ns).

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**Device Numbers**

- By varying the design of Fig. 1.10 manufacturers can alter the number of inputs and the logic function. With only few exceptions, the multiple-emitter inputs and the totem-pole outputs are used for different TTL devices. Table 1.2 lists some of the 7400 series TTL gates. For instance, the 7400 is a chip with four 2-input NAND gates in one package. Similarly, the 7402 has four 2-input NOR gates, the 7404 has six inverters, and so on.

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| *Device Number* | *Description* |
|---|---|
| 7400 | Quad 2-input NAND gates |
| 7402 | Quad 2-input NOR gates |
| 7404 | Hex inverter |
| 7408 | Quad 2-input AND gates |
| 7410 | Triple 3-input NAND gates |
| 7411 | Triple 3-input AND gates |
| 7420 | Dual 4-input NAND gates |
| 7421 | Dual 4-input AND gates |
| 7425 | Dual 4-input NOR gates |
| 7427 | Triple 3-input NOR gates |
| 7430 | 8-input NAND gate |
| 7486 | Quad 2-input XOR gates |

Table 1.2 Standard TTL

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**High-Speed TTL**

- The circuit of Fig. 1.10 is called standard TTL. By decreasing the resistances a manufacturer can lower the internal time constants; this decreases the propagation delay time. The smaller resistances, however, increase the power dissipation. This design variation is known as high-speed TTL. Devices of this type are numbered 74H00, 74H01, 74H02, and so on. A high-speed TTL gate has a power dissipating around 22 mW and a propagation delay time of approximately 6 ns.

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**low-Power TTL**

- By increasing the internal resistances a manufacturer can reduce the power dissipation of TTL gates. Devices of this type are called low-power TTL and are numbered 74L000, 74L01, 74L02, etc. These devices are slower than standard TTL because of the larger internal time constants. A low-power TTL gate has a power dissipation of 1 mW and a propagation delay time of about 35 ns.

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## Schottky TTL

With standard TTL, high-speed TTL, and low- power TTL, the transistors are switched on with excessive current, causing a surplus of carriers to be stored in the base. When you switch a transistor from on to off, you have to wait for the extra carriers to flow out of the base. The delay is known as *saturation delay time*. One way to reduce saturation delay time is with Schottky TTL.

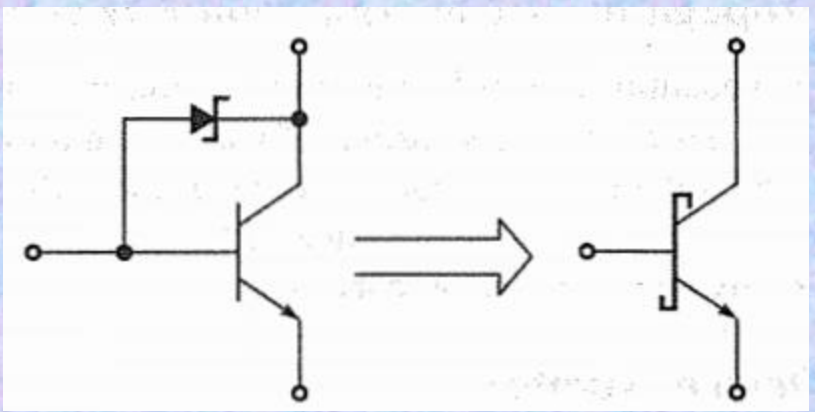

Fig. 1.11 Schottky diode prevents transistor saturation

The idea is to fabricate a Schottky diode along with each bipolar transistor of a TTL circuit, as shown in Fig. 1.11. Because the Schottky diode has a forward voltage of only 0.25 to 0.4 V, it prevents the transistor from saturating fully. This virtually eliminates saturation delay time, which means better switching speed. These devices are numbered 74S00, 74S01, 74S02, and so forth. Schottky TTL devices are very fast, capable of operating reliably at 100MHz. The 74SOO has a power dissipation around 20 mW per gate and a propagation delay time of approximately 3 ns.

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**low-Power Schottky TTL**

By increasing internal resistances as well as using Schottky diodes, manufacturers have come up with a compromise between low power and high speed: low-power Schottky TTL. Devices of this type are numbered 74LS00, 74LS01, 74LS02, etc. A low-power Schottky gate has a power dissipation of around 2 mW and a propagation delay time of approximately 10 ns.

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**The Winner**

Low-power Schottky TTL is the best compromise between power dissipation and saturation delay time, moreover, low-power Schottky TTL has emerged as the favorite of digital designers. It is used for almost everything. When you must have more output current, you can fall back on standard TTL. Or, if your application requires faster switching speed, then Schottky TTL is useful. Low-power and high-speed TTL are rarely used, if at all.

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**Floating Inputs**

When a TTL input is high (ideally+5 V), the emitter current is approximately zero (Fig. 1.12a). When a TTL input is floating (unconnected, as shown in Fig. 1.12b), no emitter current is possible because of the open circuit. Therefore, a floating TTL input is equivalent to a high output. Because of this, you sometimes see unused TTL inputs left unconnected; an open input allows the rest of the gate to function properly.

There is a disadvantage to floating inputs. When you leave an input open, it acts as a small antenna. Therefore, it will pick up stray electromagnetic noise voltages. In some environments, the noise pickup is large enough to cause erratic operation of logic circuits. For this reason, most designers prefer to connect unused TTL inputs to the supply voltage.

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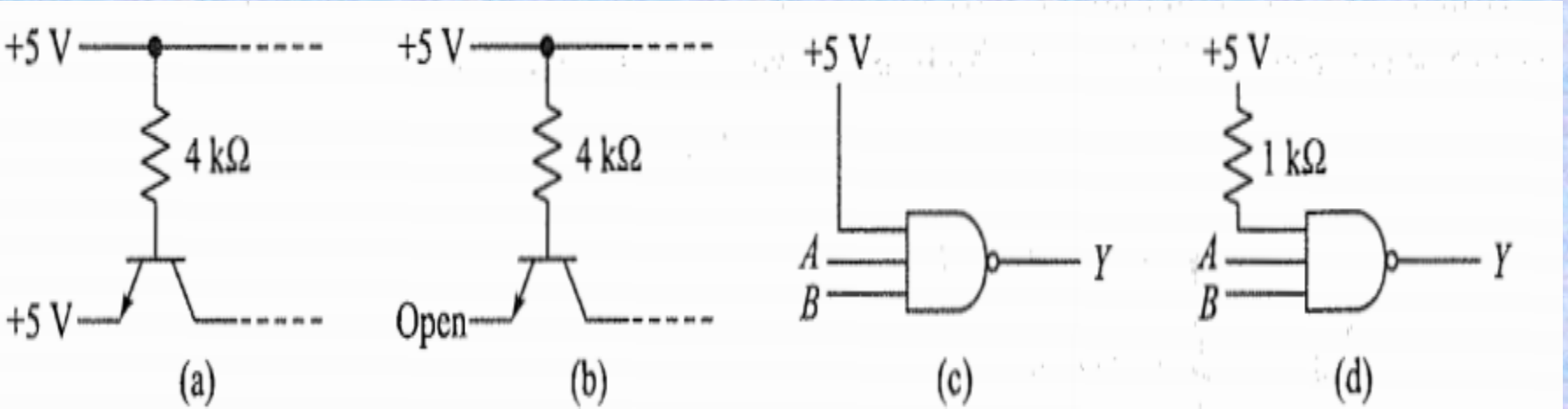


**Fig 1.12 (a) High input, (b) Open is equivalent to high input, (c) Direct connection to supply voltage, (d) High input through a pull-up resistor**

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- For instance, Fig. 1.12c shows a 3-input NAND gate. The top input is unused, so it is connected to +5 V. A direct connection like this is all right with most Schottky devices (74S and 74LS) because their inputs can withstand supply over voltages caused by switching transients. Since the top input is always high, it has no effect on the output. (Note: You don't ground the unused TTL input of Fig. 1.12c because then the output would remain stuck high, no matter what the values of A and B.)
- Figure 1.12d shows an indirect connection to the supply through a resistor. This type of connection is used with standard, low-power, and high-speed TTL devices (74, 74L, and 74H). These older TTL devices have an absolute maximum input rating of +5.5 V. Beyond this level, the ICs may be damaged. The resistor is called a pull-up resistor because it serves to pull the input voltage up to a high. Most transients on the supply voltage are too short to charge the input capacitance through the pull-up resistor. Therefore, the input is protected against temporary over voltages.

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## Worst-Case Input Voltages

- Figure 1.13a shows a TTL inverter with an input voltage of $V_i$ and an output voltage of $V_o$. When $V_i$ is 0 V (grounded), it is in the low state and is designated $V_{IL}$ With TTL devices, we can increase $V_{IL}$ to 0.8 V and still have a low-state input because the output remains in the high state. In other words, the low-state input voltage $V_{IL}$ can have any value from 0 to 0.8 V. TTL data sheets list the worst-case low input as

$$V_{IL,max} = 0.8 \text{ V}$$

- If the input voltage is greater than this, the output state is unpredictable.

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- However, suppose $V_i$ is 5 Vin Fig. 1.13a. This is a high input and can be designated $V_{IH}$, This voltage can decrease all the way down to 2 V without changing the output state. In other words, the high-stage input $V_{IH}$ is from 2 to 5 V; any input voltage in this range produces a low output voltage. Data sheets list the worst-case high input as

$$V_{IH,min} = 2 \text{ V}$$

- When the input voltage is less than this, the output state is again unpredictable.

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- Figure 1.13b summarizes these ideas. As you see, any input voltage less than 0.8 V is a valid low-state input. Any input greater than 2 V is a valid high-state input. Any input between 0.8 and 2 V is indeterminate because there is no guarantee that it will produce the correct output voltage.

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**Worst-Case Output Voltages**

- Ideally, the low output state is 0V, and the high output state is 5 V. We cannot attain these ideal values because of internal voltage drops inside TTL devices.
- For instance, when the output voltage is low in Fig. 1.13a, Q4 is saturated and has a small voltage drop across it. With TTL devices, any output voltage from 0 to 0.4 V is considered a low output and is designated $V_{OL}$. This means the low-state output $V_{OL}$ of a TTL device may have any value between 0 and 0.4 V. Data sheets list the worst-case low output as

$$V_{OL,max} = 0.4\ V$$

# Digital Electronic

- When the output is high, $Q_3$ acts as an emitter follower. Because of the voltage drop across $Q_3$, $D_1$, and the 130-Ω resistor, the output voltage will be less than supply voltage. With TTL devices, the high-state output voltage is designated $V_{OH}$; it has a value between 2.4 and 3.9 V, depending on the supply voltage, temperature, and load. TTL data sheets list the worst-case high output as

$$V_{OH,min} = 2.4 \text{ V}$$

# Digital Electronic

- Figure 1.13c summarizes the output states. As shown, any output voltage less than 0.4 V is a valid low- state output, any output voltage greater than 2.4 V is a valid high-state output, and any output between 0.4 and 2.4 V is indeterminate under worst-case conditions.

# Digital Electronic

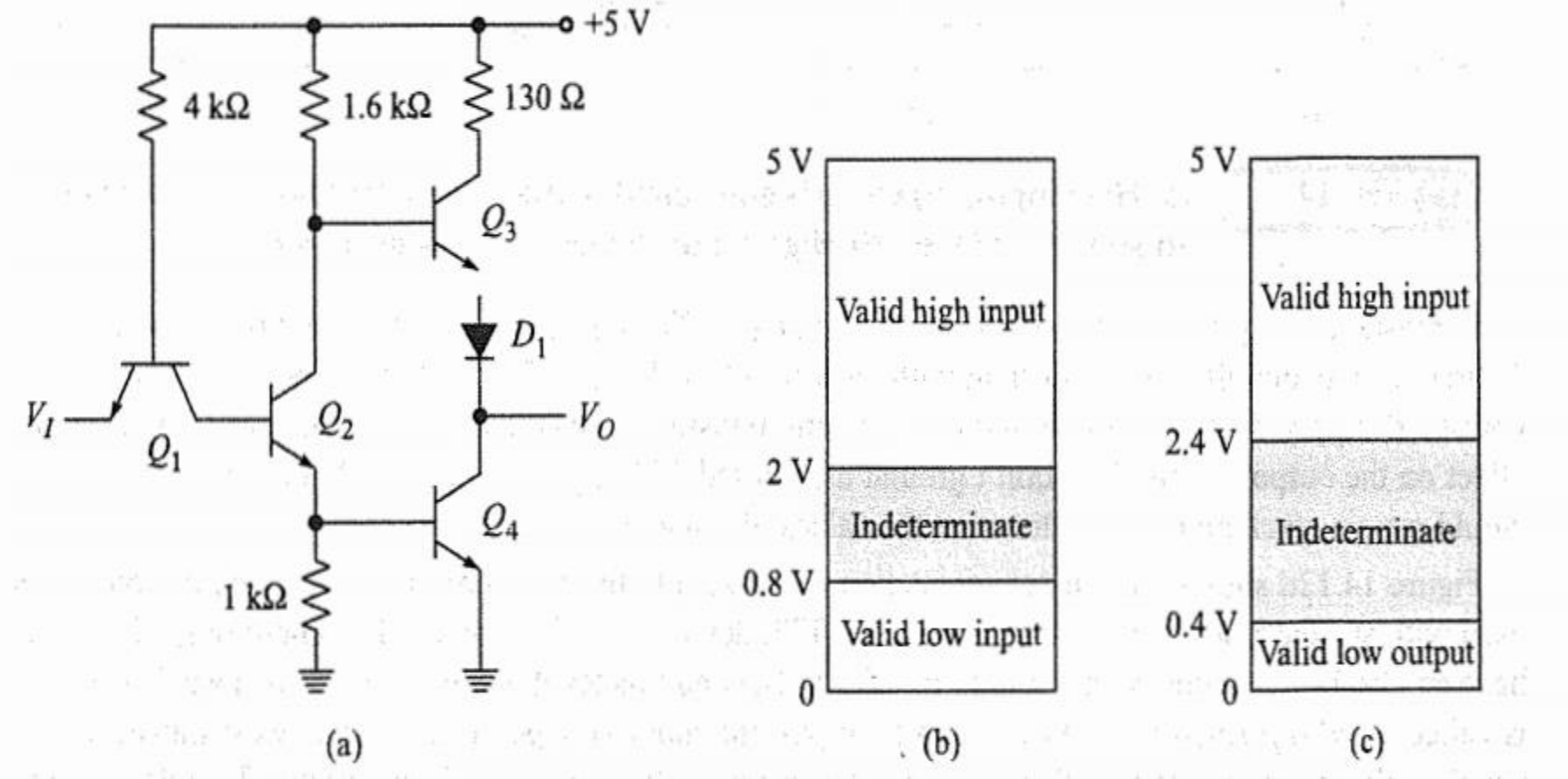



Fig. 1.13 (a) TTL inverter, (b) TTL input profile, (c) TTL output profile

# Digital Electronic

**Profiles and Windows**

- The input characteristics of Fig. 1.13b are called the TTL **input profile**. Furthermore, each rectangular area in Fig. 1.13b can be thought of as a window. There is a ***low window*** (0 to 0.8 V), an ***indeterminate window*** (0.8 to 2.0 V), and a ***high window*** (2.0 to 5 V).
- Similarly, Fig. 1.13c is the TTL **output profile**. Here you see a ***low window*** from 0 to 0.4 V, an ***indeterminate window*** from 0.4 to 2.4 V, and a ***high window*** from 2.4 to 5 V.

# Digital Electronic

## Values to Remember

- We have discussed the low and high states for the input and output voltages. Here they are again as a reference for future discussions:

$$V_{IL,\max} = 0.8\ \text{V}$$
$$V_{IH,\min} = 2\ \text{V}$$
$$V_{OL,\max} = 0.4\ \text{V}$$
$$V_{OH,\min} = 2.4\ \text{V}$$

# Digital Electronic

- These are the worst-case values shown in Fig. 1.13b and c. On the ***input side***, a voltage has to be **less** than **0.8 V** to qualify as a **low-state input**, and it must be **more** than **2 V** to be considered a **high-state input**. On the ***output side***, the voltage has to be **less** than **0.4 V** to be a **low-state output** and **more** than **2.4 V** to be a **high-state output**.

# Digital Electronic

**Compatibility**

- TTL devices are compatible because the low and high output windows fit inside the low and high input windows. Therefore the output of any TTL device is suitable for driving the input of another TTL device. For instance, Fig. 1.14a shows one TTL device driving another. The first device is called a **driver** and the second a **load**.

# Digital Electronic

- Figure 1.14b shows the output stage of the TTL driver connected to the input stage of the TTL load. The driver output is shown in the low state. Since any input less than 0.8 V is a low-state input, the driver output (0 to 0.4 V) is compatible with the load input requirements.
- Similarly, Fig. 1.14c shows high TTL output. The driver output (2.4 to 3.9 V) is compatible with the load input requirements (greater than 2 V).

# Digital Electronic

**Sourcing and Sinking**

- When a standard TTL output is low (Fig. 1.14b), an emitter current of approximately 1.6 milliamperes (mA) (worst case) exists in the direction shown. The conventional flow is from the emitter of $Q_1$ to the collector of $Q_4$. Because it is saturated, $Q_4$ acts as a current sink; conventional current flows through $Q_4$ to ground like water flowing down a sink.

# Digital Electronic

- However, when the standard TTL output is high (Fig. 1.14c), a reverse emitter current of 40 microamperes (μA) (worst-case) exists in the direction shown. Conventional current flows out of $Q_3$ to the emitter of $Q_1$. In this case, $Q_3$ is acting as a source. Data sheets list the worst-case input currents:

$$I_{IL,max} = -1.6\text{mA} \quad I_{IH,max} = 40\ \mu\text{A}$$

# Digital Electronic

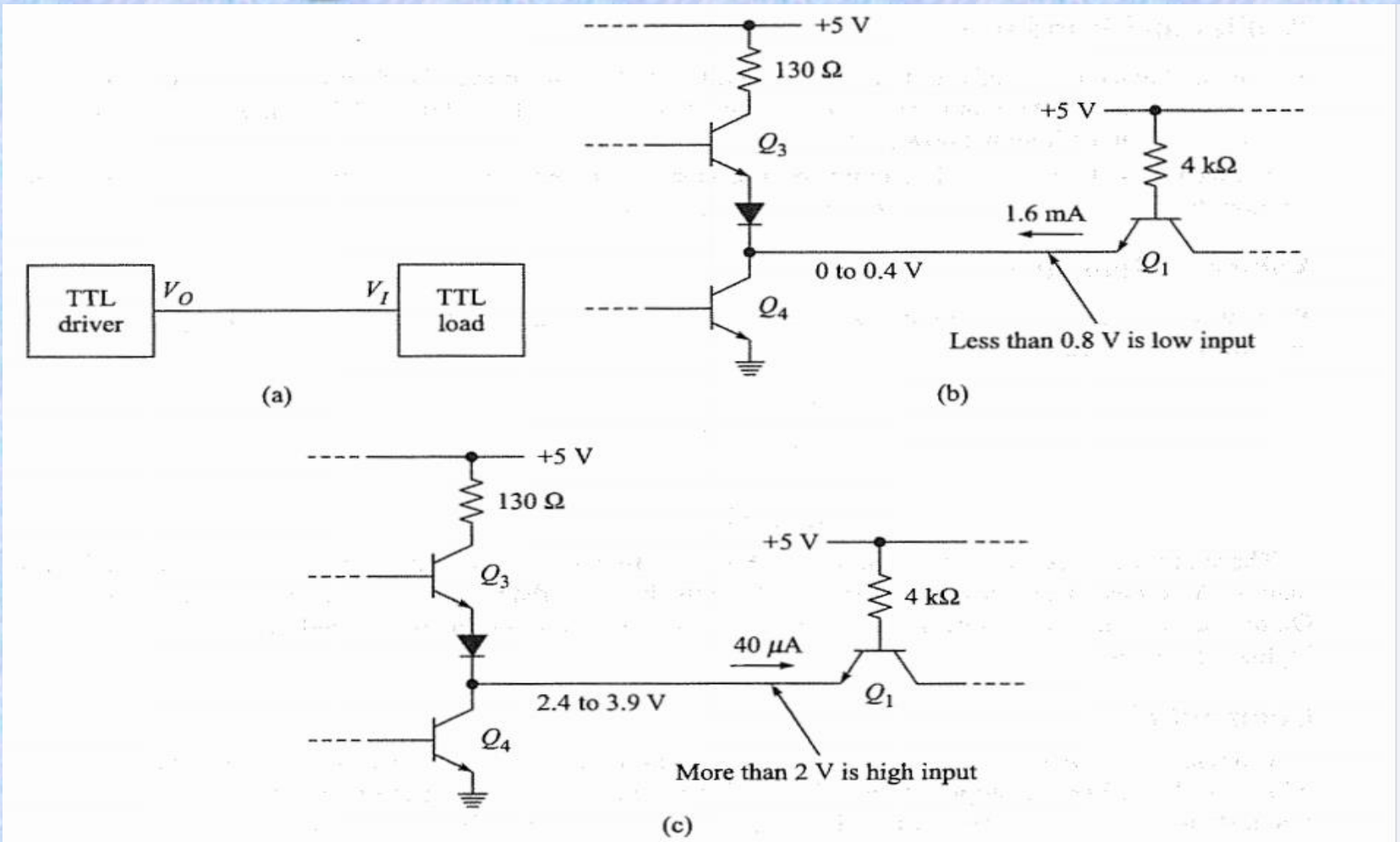



Fig. 1.14 Sourcing and sinking current

# Digital Electronic

- The minus sign indicates that the conventional. current is out of the device; a plus sign means the conventional current is into the device. AH data sheets use this notation, so do not be surprised when you see minus currents. The previous data tells us the maximum input current is 1.6 mA (outward) when an input is low and 40 μA (inward) when an input is high.

# Digital Electronic

## Noise Immunity

- In the worst case, there is a difference of 0.4 V between the **driver output** voltages and required **load input** voltages. For instance, the worst-case low values are

| | | |
|---|---|---|
| $V_{OL,\max}$ | = 0.4 V | driver output |
| $V_{IL,\max}$ | = 0.8 V | load input |

- Similarly, the worst-case high values are

| | | |
|---|---|---|
| $V_{OH,\min}$ | = 2.4 V | driver output |
| $V_{IH,\min}$ | = 2 V | load input |

# Digital Electronic

- In either case, the difference is 0.4 V. This difference is called noise immunity. It represents built-in protection against noise.
- Why do we need protection against noise? The connecting wire between a TTL driver and load is equivalent to a small antenna that picks up stray noise signals. In the worst case, the low input to the TTL load is

$$V_{IL} = V_{OL} + V_{noise} = 0.4\,V + V_{noise}$$

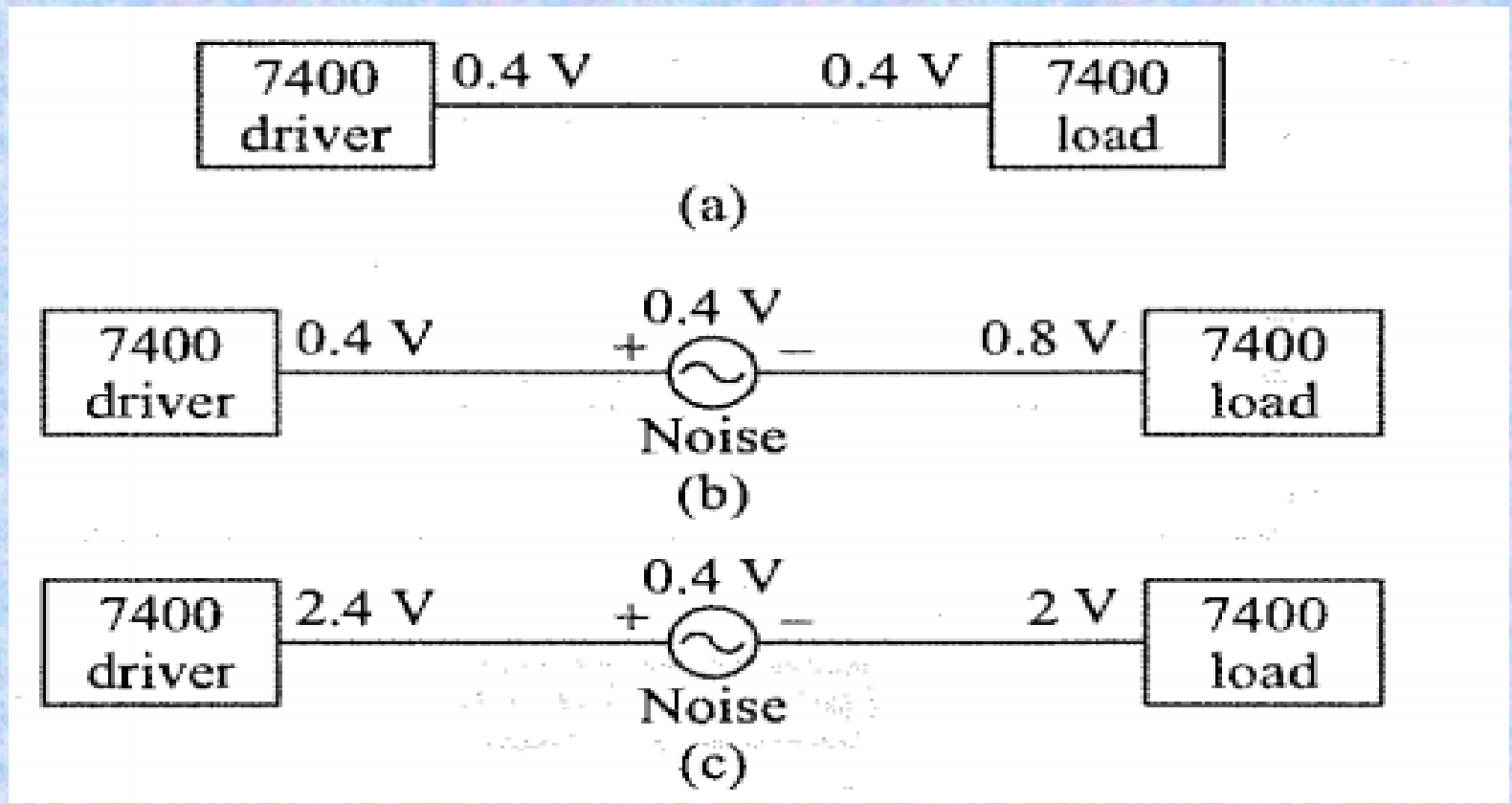
# Digital Electronic

- and the high-stage input is

$$V_{IH} = V_{OH} - V_{noise} = 2.4\,V - V_{noise}$$

- In most environments, the induced noise voltage is less than 0.4 V, and we get no false triggering of the TTL load.

# Digital Electronic




- Fig. 1.15 (a) TTL driver and load, (b) False triggering into high state, (c) false triggering into low state

# Digital Electronic

- For instance, Fig. 1.15a shows a low output from the TTL driver. If no noise voltage is induced on the connecting wire, the input voltage to the TTL load is 0.4 V, as shown. In a noisy environment, however, it is possible to have 0.4 V of induced noise on the connecting wire for either the low state (Fig. 1.15b) or the high state (Fig. 1.15c). Either way, the TTL load has an input that is on the verge of being unpredictable. The slightest additional noise voltage may produce a false change in the output state of the TTL load.

# Digital Electronic

**Standard loading**

- A TTL device can source current (high output) or sink current (low output). Data sheets of standard TTL devices indicate that any 7400 series device can sink up to 16 mA, designated

$$I_{OL,\max} = 16 \text{ mA}$$

- and can source up to 400 μA, designated

$$I_{OH,\max} = -400\ \mu\text{A}$$

# Digital Electronic

- (Again, a minus sign means that the conventional current is out of the device, and a plus sign means that it is into the device.) As discussed earlier, the worst-case TTL input currents are

$$I_{IL,\max} = -1.6\ \text{mA} \quad I_{IH,\max} = 40\ \mu\text{A}$$

- Since the maximum output currents are 10 times larger than the input currents, we can connect up to **10 TTL emitters** to any **TTL output**.

# Digital Electronic

- As an example, Fig. 1.16a shows a low output voltage (worst case). Notice that a single TTL driver is connected to 10 TTL loads (only the input emitters are shown). Here you see the TTL driver sinking 16 mA, the sum of the 10 TTL load currents. In the low state, the output voltage is guaranteed to be 0.4 V or less. If you try connecting more than 10 emitters, the output voltage may rise above 0.4 V under worst-case conditions. If this happens, the low-state operation is no longer reliable. Therefore, 10 TTL loads are the maximum that a manufacturer allows for guaranteed low-state operation.

# Digital Electronic

- Figure 1.16b shows a high output voltage (worst case) with the driver sourcing 400 μA for l0 TTL loads of 40 μA each. For this source current, the output voltage is guaranteed to be 2.4 V or greater under worst- case conditions. If you try to connect more than 10 TTL loads, you will exceed $I_{O\,H,max}$ and high-state operation becomes unreliable.

# Digital Electronic

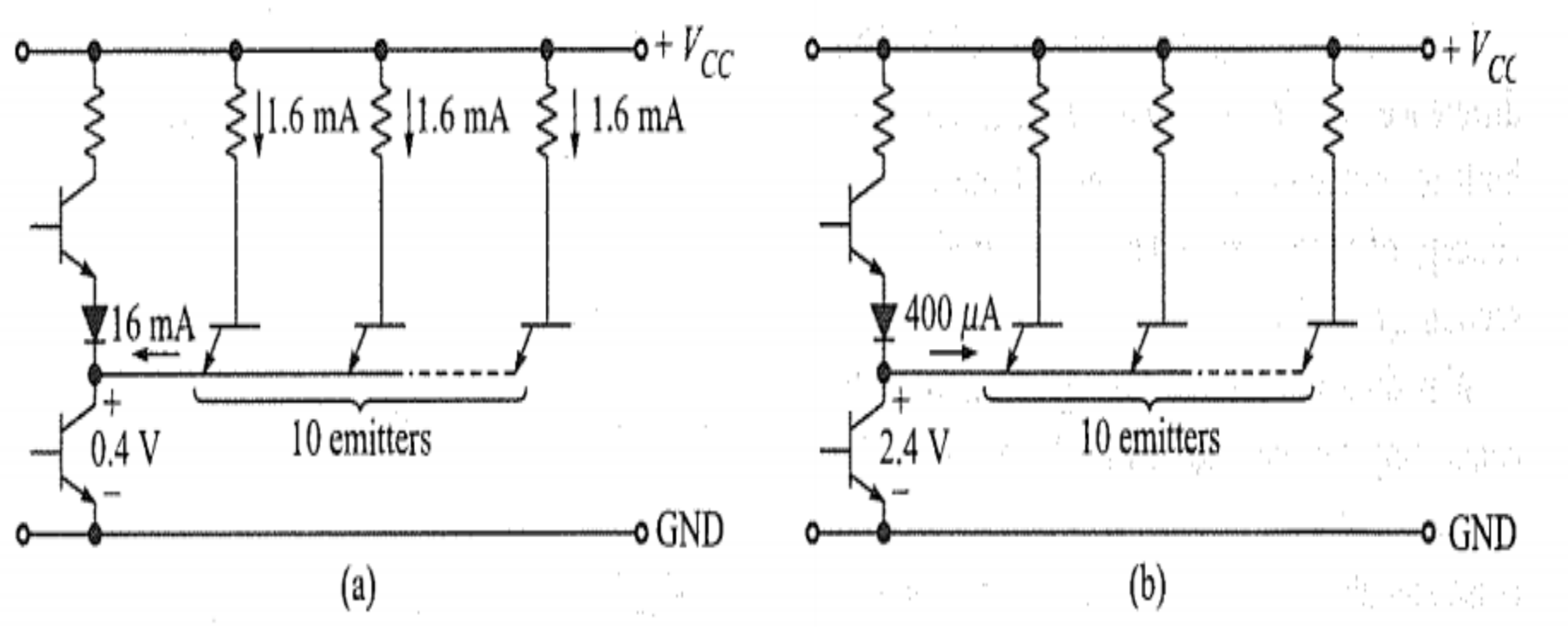


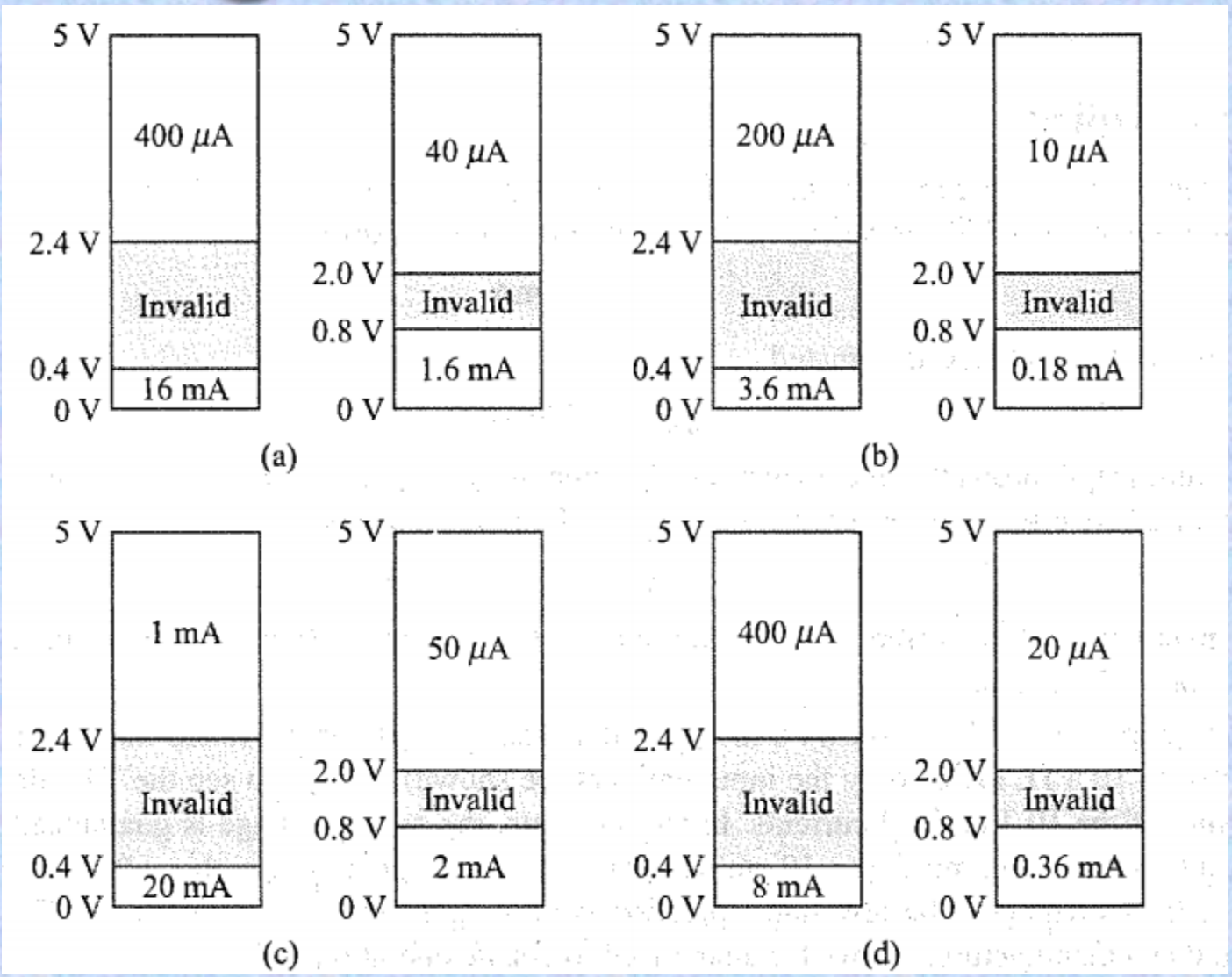

Fig. 1.16 (a) Low-state fanout, (b) High-state fanout

# Digital Electronic

**Loading Rules**

- Figure 1.17 shows the output-input profiles for different types of TTL. The output profiles are on the left, and the input profiles are on the right. These profiles are a concise summary of the voltages and currents for each TTL type. Start with the profiles of Fig. 1.17a; these are for standard TTL. On the left, you see the profile of output characteristics. The high output window is from 2.4 to 5 V with up to 400 μA of source current; the low output window is from 0 to 0.4 V with up to 16 mA of sink current. On the right, you see the input profile of a standard TTL device. The high window is from 2 to 5 V with an input current of 40 μA, while the low window is from 0 to 0.8 V with an input current of 1.6 mA.

# Digital Electronic




- Fig. 1.17 TTL output-input profiles: (a) Standard TTL, (b) Low-power TTL, (c) Schottky TTL, (d) Low-power Schottky TTL

# Digital Electronic

- Standard TTL devices are compatible because the low and high output windows fit inside the corresponding input window. In other words, 2.4 V is always large enough to be a high input to a TTL load, and 0.4 V is always small enough to be a low input. Furthermore, you can see at a glance that the available source current is 10 times the required high-state input current, and the available sink current is 10 times the required low-state input current. **The maximum number of TTL loads that can be reliably driven under worst-case conditions is called the fanout**. With standard TTL, the fanout is 10 because one TTL driver can drive I0 TTL loads.

# Digital Electronic

- The remaining figures all have identical voltage windows. The output states are always 0 to 0.4 and 2.4 to 5 V, while the input states are 0 to 0.8 and 2 to 5 V. For this reason, all the TTL types are compatible; this means you can use one type of TTL as a driver and another type as a load.

# Digital Electronic

- The only differences in the TTL types are the currents. You can see in Fig. 1.17a to d that the input and output currents differ for each TTL type. For instance, a low-power Schottky TTL driver (see Fig. 1.17d) can source 400 μA and sink 8 mA; a low-power Schottky load requires input currents of 20 μA (high state) and 0.36 mA (low state). These numbers are different from standard TTL (Fig. 1.17a) with its output currents of 400 μA and 16 mA and its input currents of 40 μA and 1.6 mA.

# Digital Electronic

- Incidentally, notice that the profiles of high-speed TTL are omitted in Fig. 1.17 because Schottky TTL has replaced high-speed TTL, in virtually all applications. If you need high-speed TTL data, consult manufacturers' catalogs.
- By analyzing Fig. 1.17a to d (plus the data sheets for high-speed TTL), we can calculate the fanout for all possible combinations. Table 1.3 summarizes these fanouts, which are useful if you ever have to mix TTL types.

# Digital Electronic

- Read Table 1.3 as follows. The TTL types have been abbreviated; 74 stands for 7400 series (standard), 74H for 74H00 series (high speed), and so forth. Drivers are on the left, and loads are on the 1ight. Pick the driver, pick the load, and read the fanout at the intersection of the two. For instance, the fanout ofa standard device (74) driving low-power Schottky devices (74LS) is 20. As another example, the fanout of a low-power device (74L) driving high-speed devices (74H) is only 1.

# Digital Electronic

| TTL Driver | TTL Load | | | | |
|---|---|---|---|---|---|
| | 74 | 74H | 74L | 74S | 74LS |
| 74 | 10 | 8 | 40 | 8 | 20 |
| 74H | 12 | 10 | 50 | 10 | 25 |
| 74L | 2 | 1 | 20 | 1 | 10 |
| 74S | 12 | 10 | 100 | 10 | 50 |
| 74LS | 5 | 4 | 40 | 4 | 20 |

Table 1.3 Fanouts

# Digital Electronic

## OPEN-COLLECTOR GATES

- Instead of a totem-pole output, some TTL devices have an open-collector output. This means they use only the lower transistor of a totem-pole pair. Figure 1.22a shows a 2-input NAND gate with an open-collector output. Because the collector of $Q_4$ is open, a gate like this will not work properly until you connect an external pull-up resistor, shown in Fig. 1.22b.
- The outputs of open-collector gates can be wired together and connected to a common pull-up resistor. For instance, Fig. 1.22c shows three TTL devices connected to the pull-up resistor.

# Digital Electronic

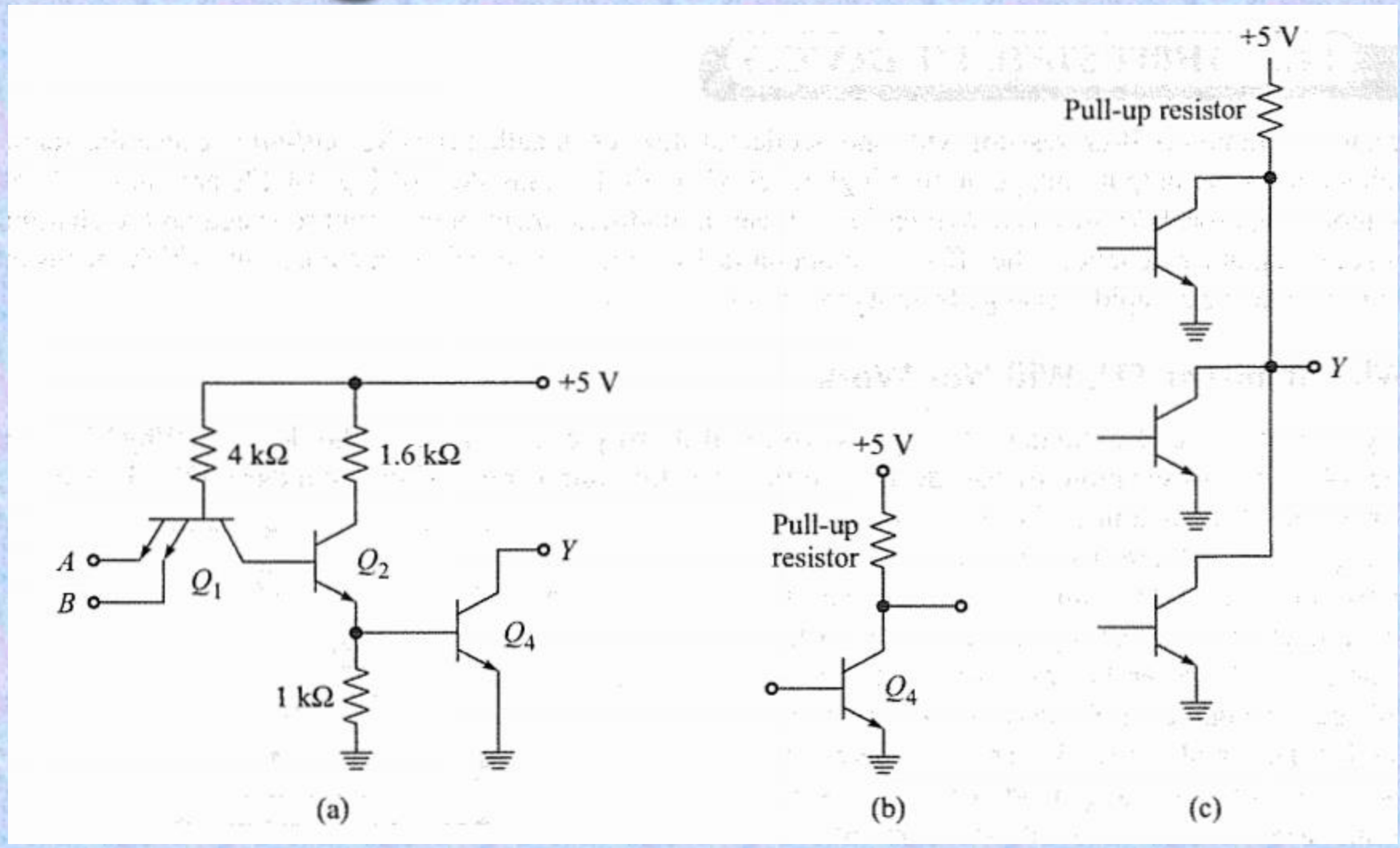



**Fig. 1.22 Open-collector TTL: (a) Circuit, (b) Pull-up resistor, (c) Open-collector outputs connected to a pull-up resistor**

# Digital Electronic

- The big disadvantage of open-collector gates is their slow switching speed. Why is it slow? Because the pull-up resistance is a few kilohms, which results in a relatively long time constant when it is multiplied by the stray output capacitance. The slow switching speed of open-collector TTL devices is worst when the output goes from low to high. Imagine all three transistors going into cutoff in Fig.1.22c. Then any capacitance across the output has to charge through the pull-up resistor. This charging produces a relatively slow exponential rise between the low and high state.

# Digital Electronic

## 1.3 THREE-STATE TTL DEVICES

- If you try to wire-OR standard TTL gates, you will destroy one or more of the devices. Why? Look at Fig. 1.23 for an example of bad design. Notice that the output pins of two standard TTL devices are connected. If the output of the second device is low, $Q_4$ is on and appears approximately like a short circuit. If, at the same time, the output of the first device is in the high state, then $Q_1$ acts as an emitter follower that tries to pull the output and $Q_4$ are both voltage to a high level. Since $Q_1$ conducting heavily, only 130 $\Omega$ remains between the supply voltage and ground. The final result is an excessive current that destroys one of the TTL devices.

# Digital Electronic

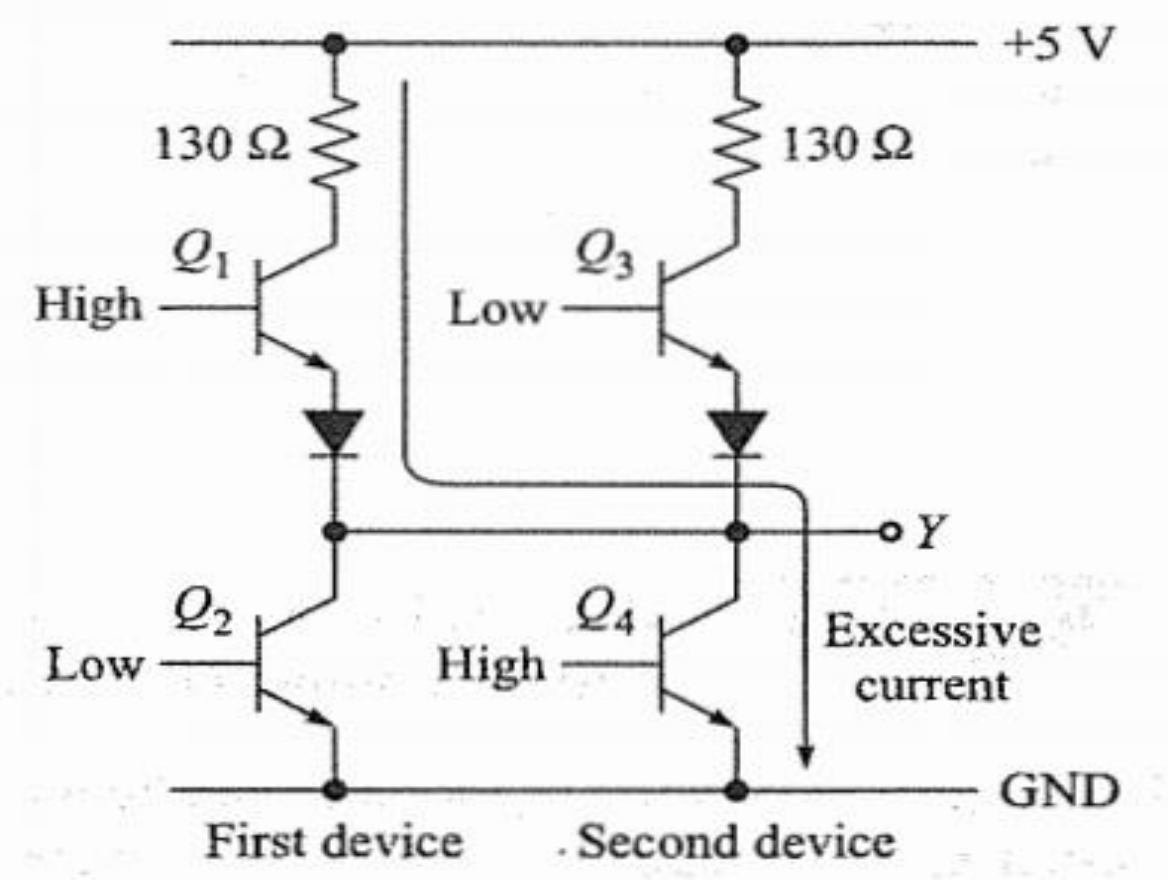



Fig. 1.23 Direct connection of TTL outputs produces excessive current

# Digital Electronic

**low DISABLE Input**

- As you have seen, wire-ORing standard TTL devices will not work because of destructive currents in the output stages.
- This inability to wire-OR ordinary totem-pole devices is what led to three-state (tri-state) TTL, a new breed of totem-pole devices introduced in the early 1970s.
- With three-state gates, we can connect totem-pole outputs directly without destroying any devices. The reason for wanting to use totem-pole outputs is to avoid the loss of speed that occurs with open-collector devices.

# Digital Electronic

- Figure 1.24 shows a simplified drawing for a three- state inverter. When DISABLE is low, the base and collector of $Q_6$ are pulled low. This cuts off $Q_7$ and $Q_8$ . Therefore, the second emitter of $Q_1$ and the cathode of $D_1$ are floating. For this condition, the rest of the circuit acts as an inverter: a low A input forces $Q_2$ and $Q_5$ to cut off, while $Q_3$ and $Q_4$ tum on, producing a high output. On the other hand, a high A input forces $Q_2$ to turn on, which drives $Q_5$ on and produces a low output.

# Digital Electronic

- Table 14.5 summarizes the operation for low DISABLE.

| *Disable* | *A* | *Y* |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | *X* | Hi-Z |

Table 1.5 Three-State Inverter

# Digital Electronic

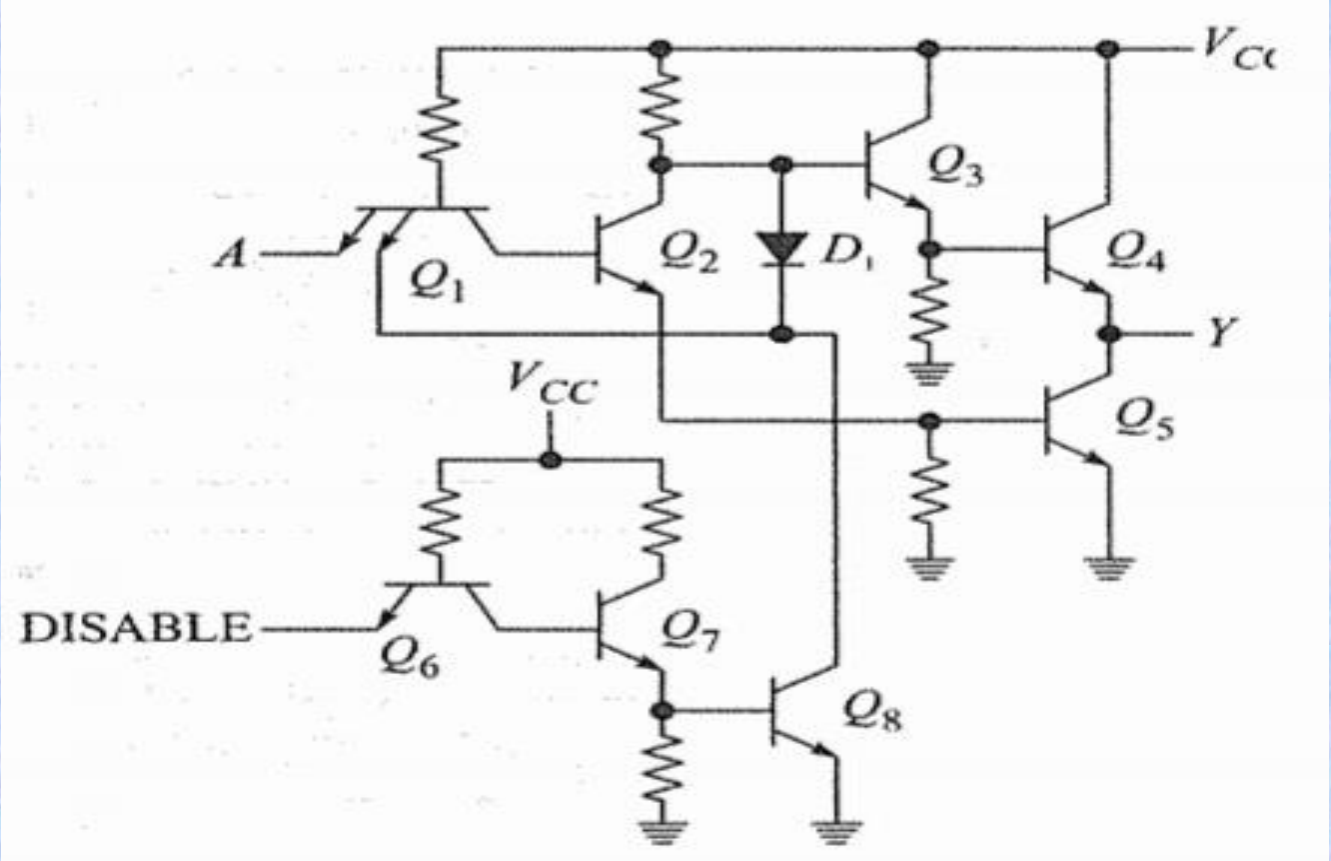



Fig. 1.24 Three-State Inverter

# Digital Electronic

High DISABLE Input

- When DISABLE is high, the base and collector of $Q_6$ go high, which turns on $Q_7$ and $Q_8$ . Ideally, the collector of $Q_8$ is pulled down to ground. This causes the base and collector of $Q_1$ to go low, cutting off $Q_2$ and $Q_5$.
- Also $Q_3$ is off because of the clamping action of $D_1$.

# Digital Electronic

- In other words, the base of $Q_3$ is only 0.7 V above ground, which is insufficient to turn on $Q_3$ and $Q_4$.
- With both $Q_4$ and $Q_5$ off, the Y output is floating. Ideally, this means that the Thevenin impedance looking back into the Y output approaches infinity. Table 1.5 summarizes the action for this high-impedance state. As shown, when DISABLE is high, input A is a don't care because it has no effect on the Y output. Furthermore, because of the high output impedance, the output line appears to be disconnected from the rest of the gate. In effect, the output line is floating.

# Digital Electronic

- In conclusion, the output of Fig. 1.24 can be in one of three states: low, high, or floating.

**Logic Symbol**

- Figure 1.25a is an equivalent circuit for the three- state inverter. When DISABLE is low, the switch is closed and the circuit acts as an ordinary inverter. When DISABLE is high, the switch is open and the Y output is floating or disconnected.

# Digital Electronic

- Figure 14.25b shows the logic symbol for a three-state inverter. When you see this symbol, remember that a low DISABLE results in normal inverter action, but a high DISABLE floats the Y output.

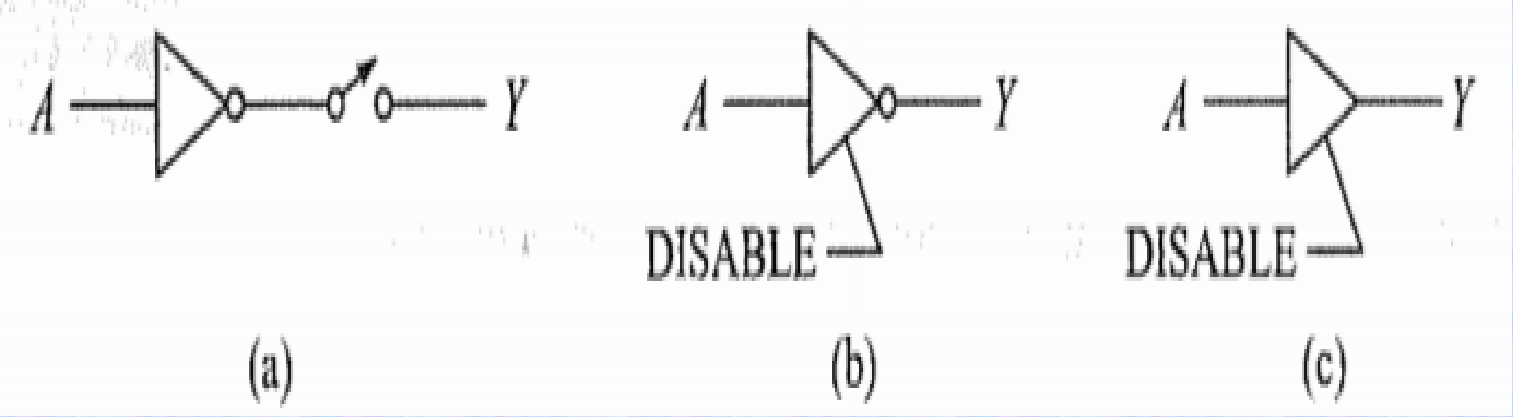



Fig. 1.25 Three-state logic diagrams: (a) Equivalent circuit of inverter, (b) logic symbol of inverter, (c) logic symbol of buffer

# Digital Electronic

**Three-State Buffer**

- By modifying the design, we can produce a three-state buffer, whose logic symbol is shown in Fig. 1.25c. When DISABLE is low, the circuit acts as a noninverting buffer, so that Y = A. But when DISABLE is high, the output floats. The three-state buffer is equivalent to an ordinary switch. When DISABLE is low, the switch is closed. When DISABLE is high, the switch is open.
- The 74365 is an example of a commercially available three-state hex noninverting buffer. This IC contains six buffers with three-state outputs. It is ideal for organizing digital components around a bus, a group of wires that transmits binary numbers between registers.

# Digital Electronic

**Bus Organization**

- Figure 1.26 shows some registers connected to a common bus. The three-state buffers control the flow of binary data between the registers. For instance, if we want the contents of register A to appear on the bus, all we have to do is make DISABLE low for register A but high for registers B and C. Then all the three-state switches on register A are closed, while all other three-state switches are open. As a result, only the contents of register A appear on the bus.

# Digital Electronic

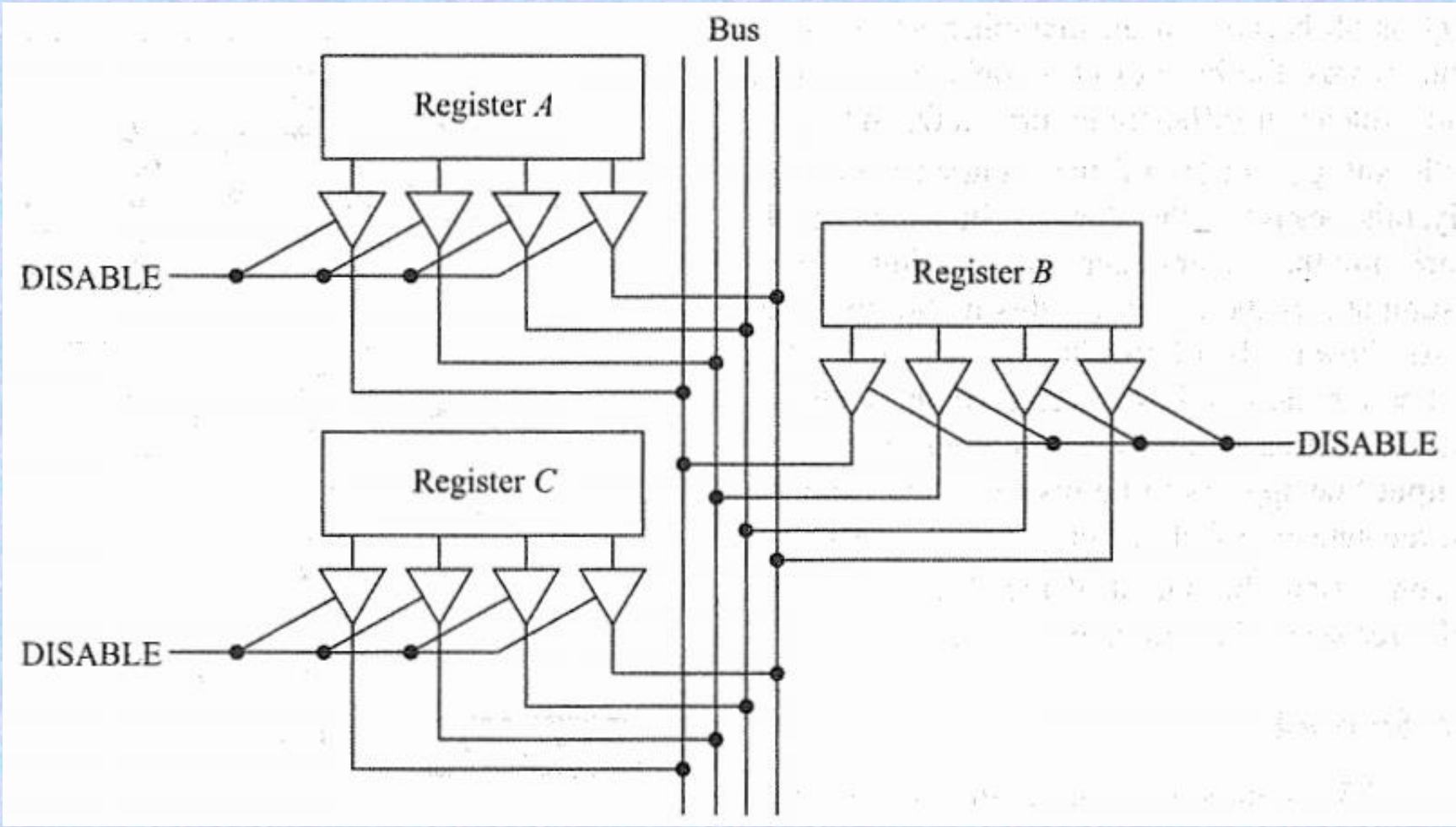



Fig. 1.26 Three-state bus control

# Digital Electronic

- The idea in any bus-organized system is to make DISABLE high for all registers except the register whose contents are to appear on the bus. In this way, dozens of registers can time-share the same transmission path. Not only does this reduce the amount of wiring, but also it has simplified the architecture and design of computers and other digital systems.

# Digital Electronic

## 1.4 TTL Driving External Loads

- Because standard TTL can sink up to 16 mA, you can use a TTL driver to control an external load such as a relay, an LED, etc. Figure 1.27 a illustrates the idea. When the TTL output is high, there is no load current. But when the TTL output is low, the lower end of RL is ideally grounded. This sets up a load current of approximately

$$I_L = \frac{5\ V}{R_L}$$

# Digital Electronic

- Since standard TTL can sink a maximum of 16 mA, the load resistance is limited to a minimum value of about

$$R_L = \frac{5\ V}{16\ mA} = 312\ \Omega$$

**Driving an LED**

- Figure 1.27b is another example. Here a TTL circuit drives an LED. When the TTL output is high, the LED is dark. When the TTL output is low, the LED lights up. If the LED voltage drop is 2 V, the LED current for a low TTL output is approximately

$$I_L = \frac{5\ V - 2\ V}{270\ \Omega} = 1.11\ mA$$

# Digital Electronic

**Supply Voltage Different from +5 V**

- If you need to use a supply voltage different from +5 V, you can use an open-collector TTL device. For instance, Fig. 1.28a on the next page shows an open-collector gate driving a load resistor that is returned to +15 V. Since an open-collector device can sink a maximum of 16 mA, the minimum load resistance in Fig. 1.28a is slightly less than 1 kΩ.

# Digital Electronic

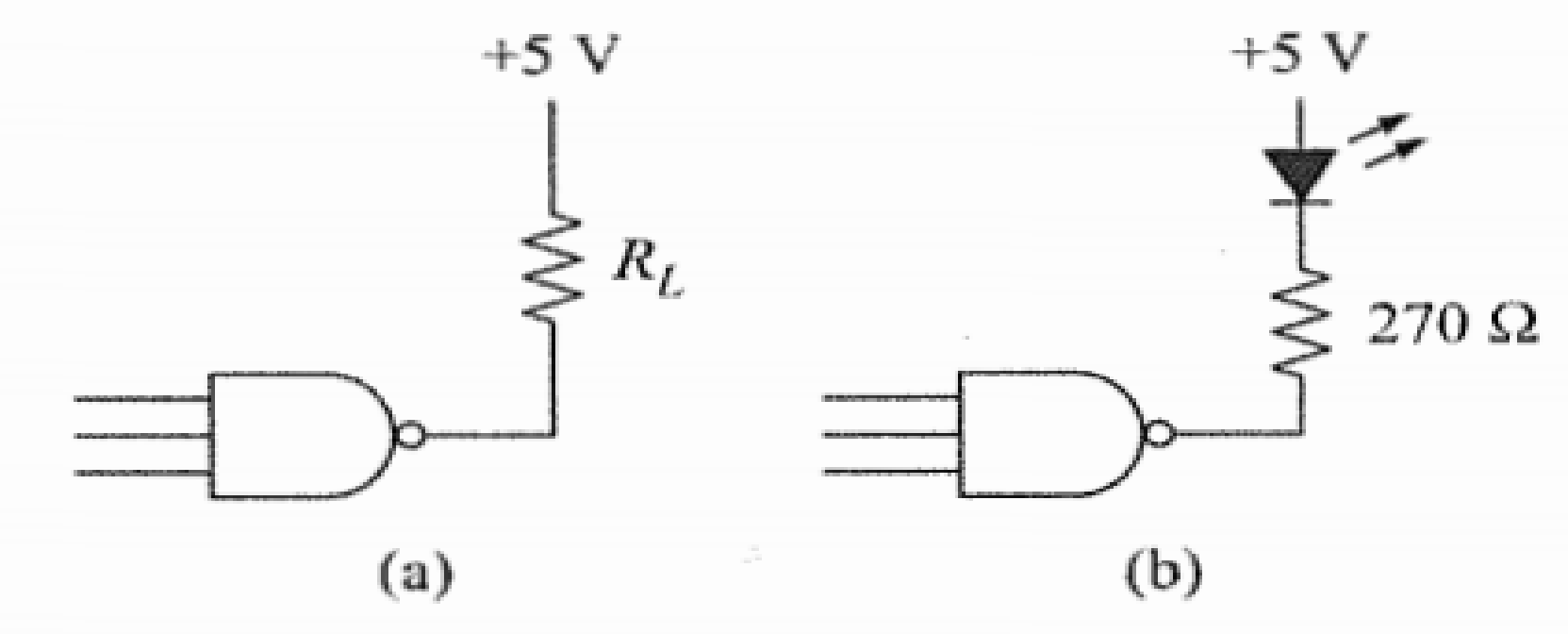



Fig. 1.27 (a) TTL output drives load resistor, (b) TTL output drives LED.

# Digital Electronic

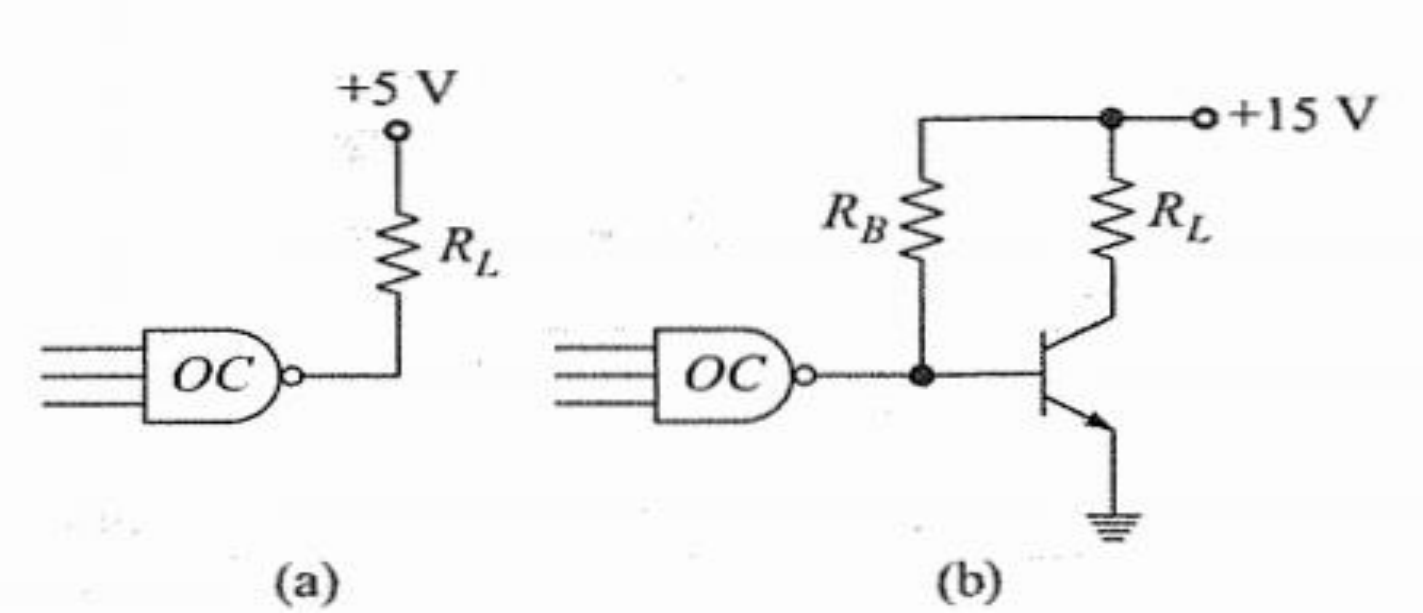



Fig 1.28 (a) Open-collector device allows a higher supply voltage, (b) Transistor increases current drive

# Digital Electronic

- If you want more than 16 mA of load current, you can use an external transistor, as shown in Fig. 1.28b.
- When the open-collector device has a low output, the external transistor goes off and the load current is zero.
- When the device has a high output, the external transistor goes on and the load current is maximum.

# Digital Electronic

## 1.5 74C00 CMOS

- National Semiconductor Corporation pioneered the 74COO series, a line of CMOS circuits that are pin-for-pin and function-for-function compatible with TTL devices of similar numbers.
- For instance, the 74COO is a quad 2-input NAND gate, the 74C02 is a quad 2-input NOR gate, and so on. This CMOS family contains a variety of small-scale integration (SSI) and medium-scale integration (MSI) chips that allow you to replace many TTL designs by the comparable CMOS designs.
- This is useful if you are trying to build battery-powered equipment. The 74HCOO series is the high-speed CMOS family.

# Digital Electronic

**NAND Gate**

- Figure 1.29 shows a CMOS NAND gate. The complementary design of input and output stages is typical of CMOS devices. Notice that $Q_1$ and $Q_2$ form one complementary connection; $Q_3$ and $Q_4$ form another; Visualize these transistors as switches. Then a low A input will close $Q_1$ and open $Q_2$; a high A input will open $Q_1$ and close $Q_2$. Similarly, a low B input will open $Q_3$, and close $Q_4$ ; a high B input will close $Q_3$ and open $Q_4$.

# Digital Electronic

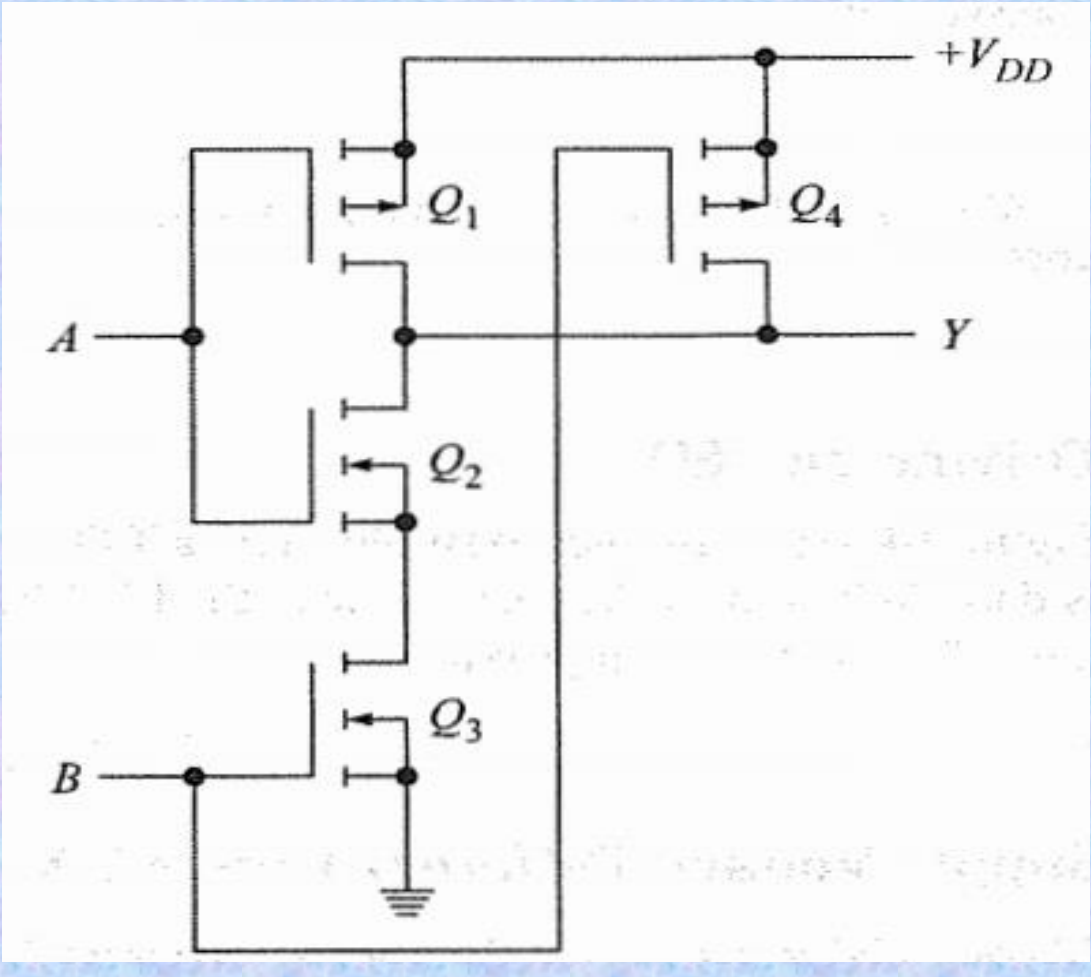



Fig. 1.29 CMOS NAND gate

# Digital Electronic

- In Fig. 1.29, the Y output is pulled up to the supply voltage when either $Q_1$ or $Q_4$ is conducting. The output is pulled down to ground only when $Q_2$ and $Q_3$ are conducting. If you keep this in mind, it simplifies the following discussion.

1- **Case 1** Here A is low and B is low. Because A is low, $Q_1$ is closed. Therefore, Y is pulled high through the small resistance of $Q_1$.

# Digital Electronic

2- **Case 2** Now A is low and B is high. Since A is still low, $Q_1$ remains closed and Y stays in the high state.

3- **Case 3** The A input is high and the B is low. Because B is low, $Q_4$ is closed. This pulls Y up to the supply voltage through the small resistance of $Q_4$.

4- **Case 4** The A is high, and the B is high. When both inputs are high, $Q_2$ and $Q_3$ are closed, pulling the output down to ground.

# Digital Electronic

- Table 1.6 summarizes all input-output possibilities. As you can see, this is the truth table of a positive NAND gate. The output is low only when all inputs are high. To produce the positive AND function, we can connect the output of Fig. 1.29 to a CMOS inverter.

Table 1.6
CMOS NAND Gate

| *A* | *B* | *Y* |
|---|---|---|
| Low | Low | High |
| Low | High | High |
| High | Low | High |
| High | High | Low |

# Digital Electronic

**NOR Gate**

- Figure 1.30 shows a CMOS NOR gate. The output goes high only when $Q_1$ and $Q_2$ are closed. The output goes low if either Q or Q is closed. There are four possible cases:

1- **Case 1** The A is low, and the B is low. For both inputs low, $Q_1$ and $Q_2$ are closed. Therefore, Y is pulled high though the small series resistance of $Q_1$ and $Q_2$.

# Digital Electronic

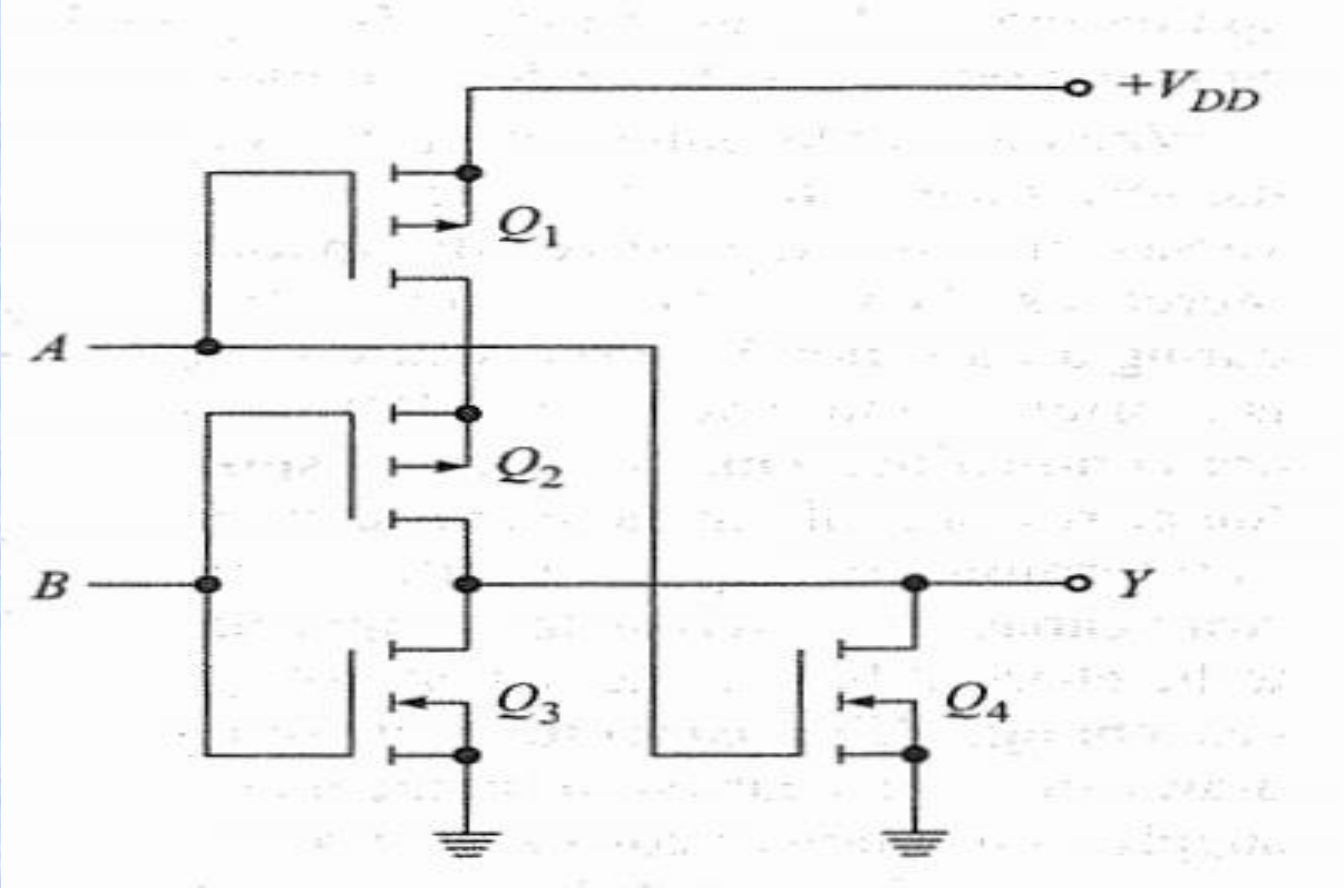



Fig. 1.30 CMOS NOR gate

# Digital Electronic

2- **Case 2** The A is low, and the B is high. Because B is high, $Q_3$ is closed, pulling the output down to ground.

3- **Case 3** The A is high, and the B is low. With A high, $Q_4$ is closed. The closed $Q_4$ pulls the output low.

4- **Case 4** The A is high, and the B is high. Since A is still high, $Q_4$ is still closed and the output remains low.

# Digital Electronic

- Table 1.7 summarizes these possibilities. As you can see, this is the truth table of a positive NOR gate. The output is low when any input is high.

| *A* | *B* | *Y* |
|---|---|---|
| Low | Low | High |
| Low | High | Low |
| High | Low | Low |
| High | High | Low |

Table 1.7

# Digital Electronic

**Propagation Delay Time**

- A standard CMOS gate has a propagation delay time $t_p$ of approximately 25 to 100 ns, with the exact value depending on the power supply voltage and other factors. As you recall, $t_p$ is the time it takes for the output of a gate to change after its inputs have changed. When two or more CMOS gates are cascaded, you have to add the propagation delay times to get the total. For instance, if you cascade three CMOS gates each with a tp of 50 ns, then the total propagation delay time is 150 ns.

# Digital Electronic

**Power Dissipation**

- The ***static power*** dissipation of a device is its average power dissipation when the output is constant. The static power dissipation of a CMOS gate is in nanowatts. For instance, a 74C00 has a power dissipation of approximately 10 nanowatts (nW) per gate. This dissipation equals the product of supply voltage and leakage current, both of which are dc quantities.

# Digital Electronic

- When a CMOS output changes from the low state to the high state (or vice versa), the average power dissipation increases. Why? The reason is that during a transition between states, there is a brief period when both MOSFETs are conducting. This produces a spike (quick rise and fall) in the supply current.

# Digital Electronic

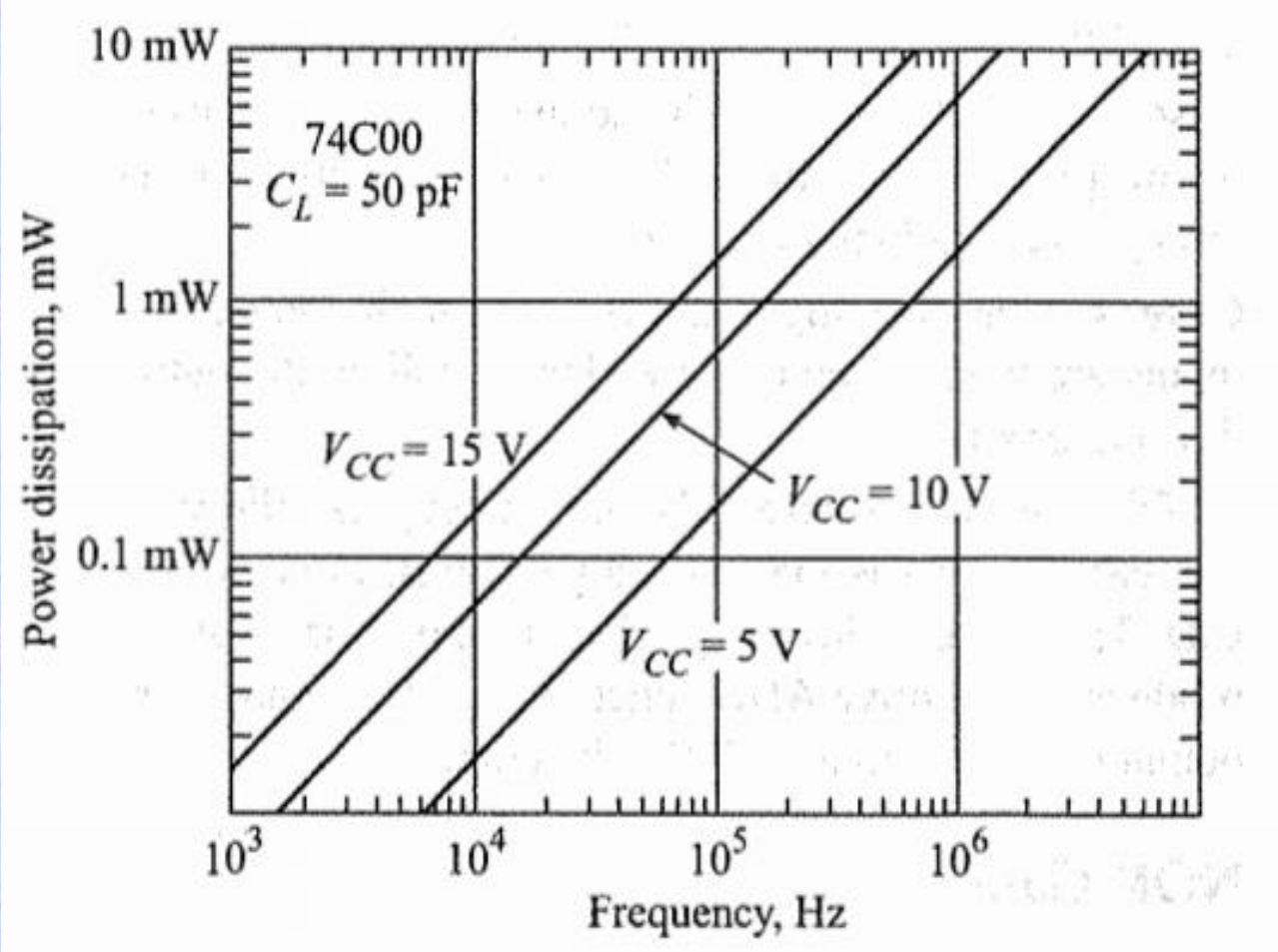
- Furthermore, during a transition, any stray capacitance across the output has to be charged before the output voltage can change. This capacitive charging draws additional current from the power supply. Since power equals the product of supply voltage and device current, the instantaneous power dissipation increases, which means the average power dissipation is higher.

# Digital Electronic

- The average power dissipation of a CMOS device whose output is continuously changing is called the ***active power*** dissipation.
- How large is the active power dissipation?
- This depends on the frequency at which the output is switching states. When the operating frequency increases, the current spikes occur more often and active power dissipation increases. Figure 1.31 shows the active power dissipation of a 74C00 versus frequency for a load capacitance of 50pF. As you see, the power dissipation per gate increases with frequency and supply voltage. For frequencies in the megahertz region, the gate dissipation approaches or exceeds 10 mW (TTL gate dissipation). For CMOS to have an advantage over TTL, you operate CMOS devices at **lower frequencies**.

# Digital Electronic

Fig. 1.31
Active power dissipation of a 74COO



# Digital Electronic

- Another way to reduce power dissipation is to decrease the supply voltage. But this has adverse effects because it increases propagation time and decreases noise immunity. Although CMOS devices can work over a range of 3 to 15 V, the best compromise for speed, noise immunity, and overall performance is a supply voltage from 9 to 12 V. From now on, we assume a supply voltage of 10 V, unless otherwise specified.
- Incidentally, notice the use of $V_{CC}$ rather than $V_{DD}$ for the supply voltage. This is a carryover from TTL circuits. You will find $V_{CC}$ on the data sheets for 74C00 devices.

# Digital Electronic

## 1.5 CMOS CHARACTERISTICS

- 74COO series devices are guaranteed to work reliably over a temperature range of -40 to +85°C and over a supply range of3 to 15 V. In the discussion that follows, worst case means the parameters are measured under the worst conditions of temperature and voltage.

# Digital Electronic

**Floating Inputs**

- When a TTL input is floating, it is equivalent to a high input. You can use a floating TTL input to simulate a high input; but as already pointed out, it is better to connect unused TTL inputs to the supply voltage. This prevents the floating leads from picking up stray noise in the environment.
- If you try to float a CMOS input, however, not only do you set up a possible noise problem, but, much worse, you produce excessive power dissipation. Because of the insulated gates, a floating input allows the gate voltage to drift into the linear region. When this happens, excessive current can flow through push-pull stages.

# Digital Electronic

- The absolute rule with CMOS devices, therefore, is to connect all input pins. Most of or all the inputs are normally connected to signal lines. If you happen to have an input that is unused, connect it to ground or the supply voltage, whichever prevents a stuck output state.
- For instance, with a positive NOR gate you should ground an unused input. Why?
- Because returning the unused NOR input to the supply voltage forces the output into a stuck low state. On the other hand, grounding an unused NOR input allows the other inputs to control the output.

# Digital Electronic

- With a positive NAND gate, you should connect an unused input to the supply voltage. If you try grounding an unused NAND input, you disable the gate because its output will stick in the high state. Therefore, the best thing to do with an unused NAND input is to tie it to the supply voltage. A direct connection is all right: CMOS inputs can withstand the full supply voltage.

# Digital Electronic

**Easily Damaged**

- Because of the thin layer of silicon dioxide between the gate and the substrate, CMOS devices have a very high input resistance, approximately infinite. The insulating layer is kept as thin as possible to give the gate more control over the drain current. Because this layer is so thin, it is easily destroyed by excessive gate voltage.

# Digital Electronic

- Aside from directly applying an excessive gate voltage, you can destroy the thin insulating layer in more subtle ways. If you remove or insert a CMOS device into circuit while the power is on, transient voltages caused by inductive kickback and other effects may exceed the gate voltage rating. Even picking up a CMOS IC may deposit enough charge to exceed its gate voltage rating.

# Digital Electronic

- One way to protect against overvoltages is to include zener diodes across the input. By setting the zener voltage below the breakdown voltage of the insulating layer, manufacturers can prevent the gate voltage from becoming destructively high. Most CMOS ICs include this form of zener protection.

# Digital Electronic

- Figure 1.32 shows a typical transfer characteristic (input-output graph) of a CMOS inverter. When the input voltage is in the low state, the output voltage is in the high state. As the input voltage increases, the output remains in the high state until a threshold is reached. Somewhere near an input voltage of $V_{cc}/2$, the output will switch to the low state. Then any input voltage greater than $V_{cc}/2$ holds the output in the low state.

# Digital Electronic

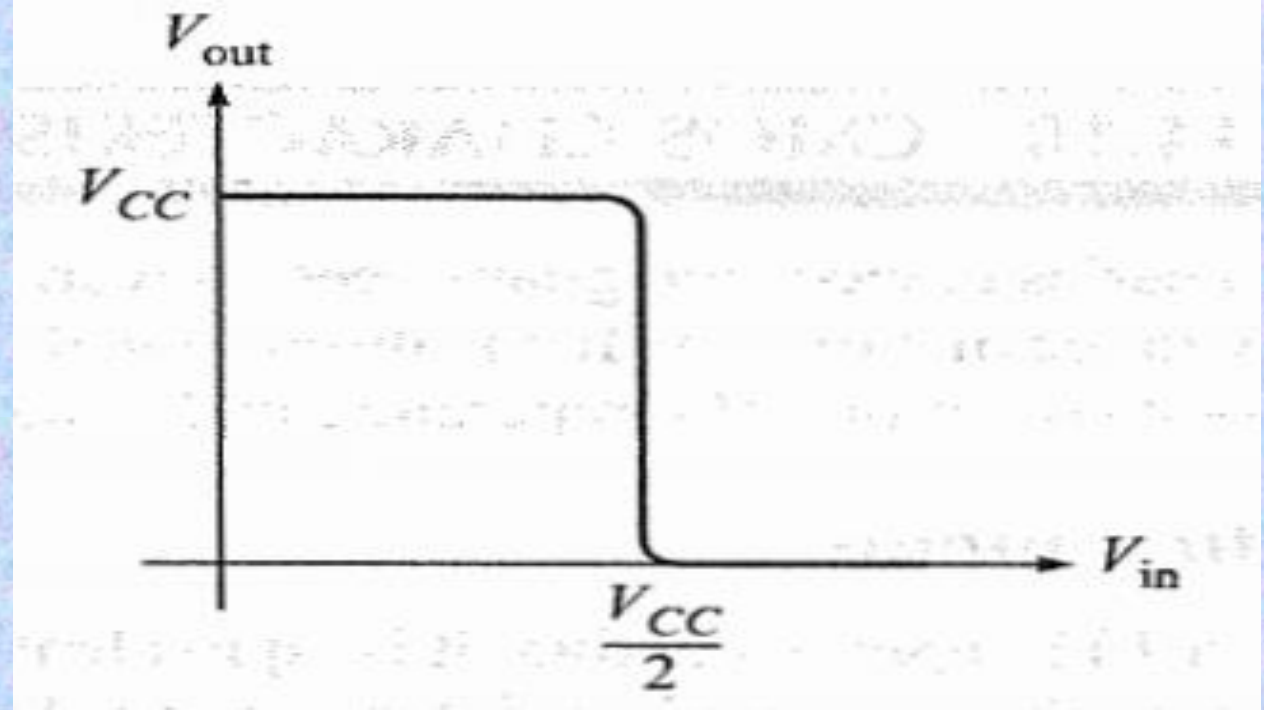



Fig. 1.32 Typical transfer characteristic of a CMOS gate

# Digital Electronic

- This transfer characteristic is an improvement over TTL. Why?
- Because the indeterminate region is much smaller. As you can see, the input voltage has to be nearly equal to $V_{CC}/2$ before the CMOS output switches states. This implies that the noise immunity of CMOS devices ideally approaches $V_{CC}/2$. Typically, noise immunity is 45 percent of $V_{CC}$.

# Digital Electronic

- Also notice how much better defined the low and high output states are. When CMOS loads are used, the CMOS source and sink transistors have almost no voltage drop because there is almost no input current to a CMOS load. Therefore, the static currents are extremely small. For this reason, the high output voltage is approximately equal to $V_{CC}$. and the low output voltage is approximately at ground.
- Stated another way, the logic swing between the **low and high** output **states** approximately equals the **supply voltage**, a considerable **advantage for CMOS over TTL**.

# Digital Electronic

**Compatibility**

- CMOS devices are compatible with one another because the output of any CMOS device can be used as the input to another CMOS device, as shown in Fig. 1.33a. For instance, Fig. 1.33b shows the output stage of a CMOS driver connected to the input stage of a CMOS load. The supply voltage is + l0V. Ideally, the input switching level is +5 V. Since the CMOS driver has a low output, the CMOS load has a high input.

# Digital Electronic

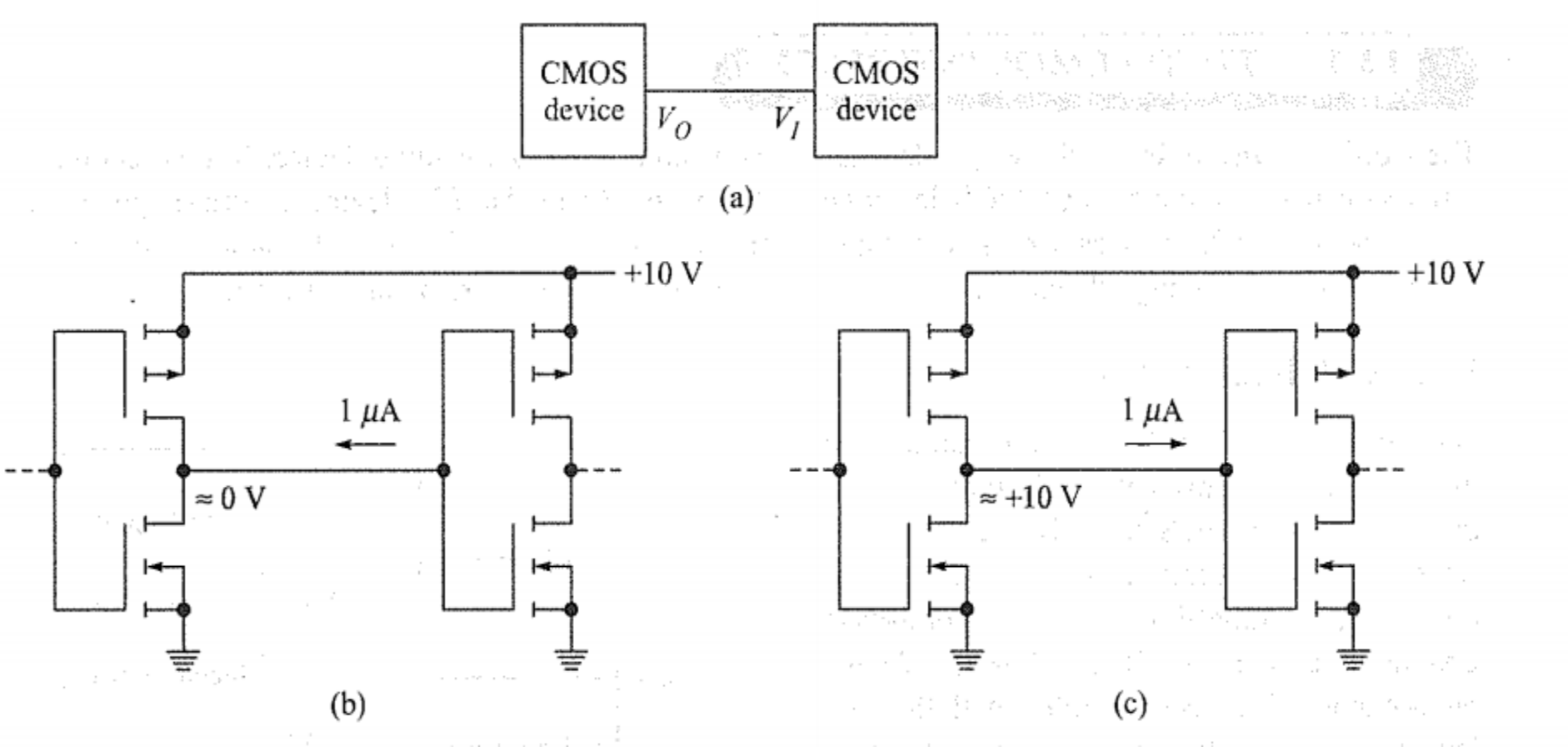



Fig1.33 (a) Output of CMOS device can drive input of another CMOS device, (b) Sink current, (c) Source current

# Digital Electronic

- Similarly, Fig. 1.33c shows a high CMOS driver output. This is more than enough voltage to drive the CMOS load with a high-state input. In fact, the noise immunity typically approaches 4.5 V (from 45 percent of $V_{CC}$.). Any noise picked up on the connecting line between devices would need a peak value of more than 4.5 V to cause unwanted switching action.

# Digital Electronic

**Sourcing and Sinking**

- When a standard CMOS driver output is low (Fig. 1.33b), the input current to the CMOS load is only 1 microampere (μA) (worst case shown on data sheet). The input current is so low because of the insulated gates. This means that the CMOS driver has to sink only 1 μA. Similarly, when the driver output is high (Fig.1.373c), the CMOS driver is sourcing 1 μA.

# Digital Electronic

- In symbols, here are the worst-case input currents for CMOS devices:

$$I_{IL,\max} = -1\ \mu\text{A} \quad I_{IH,\max} = 1\ \mu\text{A}$$

- We use these values to calculate the fanout.

# Digital Electronic

**Fanout**

- The fanout of CMOS devices depends on the kind of load being driven. In Sec. 1.6, we discuss CMOS devices driving TTL devices. Now we want to concentrate on CMOS driving CMOS. Data sheets for 74C00 series devices give the following output currents for CMOS driving CMOS:

$$I_{OL,\max} = 10\ \mu A \quad I_{OH,\max} = -10\ \mu A$$

- Since the worst-case input current of a CMOS device is only 1 μA, a CMOS device can drive up to I0 CMOS loads. Therefore, you can use a fanout of I0 for CMOS-to-CMOS connections. This value is reliable under all operating conditions.

# Digital Electronic

## 1.6 TTL-TO-CMOS INTERFACE

- The word *interface* refers to the way a driving device is connected to a loading device. In this section, we discuss methods for interfacing CMOS devices to TTL devices. Recall that TTL devices need a supply voltage of 5 V, while CMOS devices can use any supply voltage from 3 to 15 V. Because the supply requirements differ, several interfacing schemes may be used. Here are a few of the more popular methods.

# Digital Electronic

**Supply Voltage at 5 V**

- One approach to TTL/CMOS interfacing is to use +5 V as the supply voltage for both the TTL driver and the CMOS load. In this case, the worst-case TTL output voltages (Fig. 1.34a) are almost compatible with the worst-case CMOS input voltages (Fig. 1.34b). Almost, but not quite. There is no problem with the TTL low-state window (0 to 0.4 V) because it fits inside the CMOS low-state window (0 to l.5 V). This means the CMOS load always interprets the TTL low-state drive as a low.

# Digital Electronic

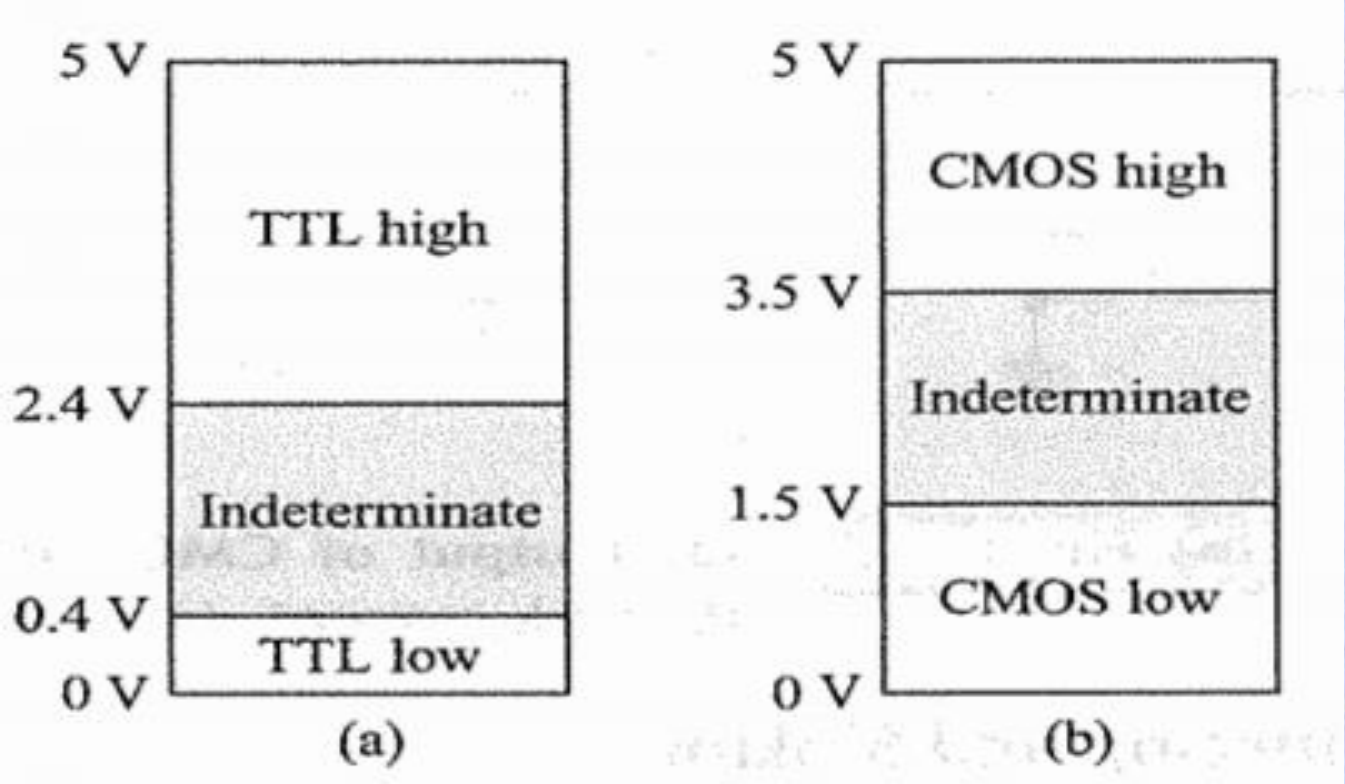



Fig. 1.34 (a) TTL output profile, (b) CMOS input profile

# Digital Electronic

- The **problem** is in the TTL **high state**, which can be as low as 2.4 V (see Fig. 1.34a). If you try using a TTL high-state output as the input to a CMOS device, you get indeterminate action.
- The CMOS device needs at least **3.5 V** for a **high-state** input (Fig. 1.34b). Because of this, you cannot get reliable operation by connecting a TTL output directly to a CMOS input. You have to do something extra to make the two different devices compatible.

# Digital Electronic

- What do you do? The standard solution is to use a pull-up resistor between the TTL driver and the CMOS load, as shown in Fig. 1.35. What effect does the pull-up resistor have? It has almost no effect on the low state, but it does raise the high state to approximately +5 V. For instance, when the TTL output is low, the lower end of the 3.3 kΩ is grounded (approximately). Therefore, the TTL driver sinks a current of roughly

# Digital Electronic

$$I = \frac{5\ \text{V}}{3.3\ \text{k}\Omega} = 1.52\ \text{mA}$$

- When the TTL output is in the high state, however, the output voltage is pulled up to +5 V. Here is how it happens. As before, the upper totem-pole transistor actively pulls the output up to +2.4 V (worst case). Because of the pull-up resistor, however, the output rises above +2.4 V, which forces the upper totem-pole transistor into cutoff. The pull-up action is now passive because the supply voltage is pulling the output voltage up to +5 V through the pull-up resistor.

# Digital Electronic

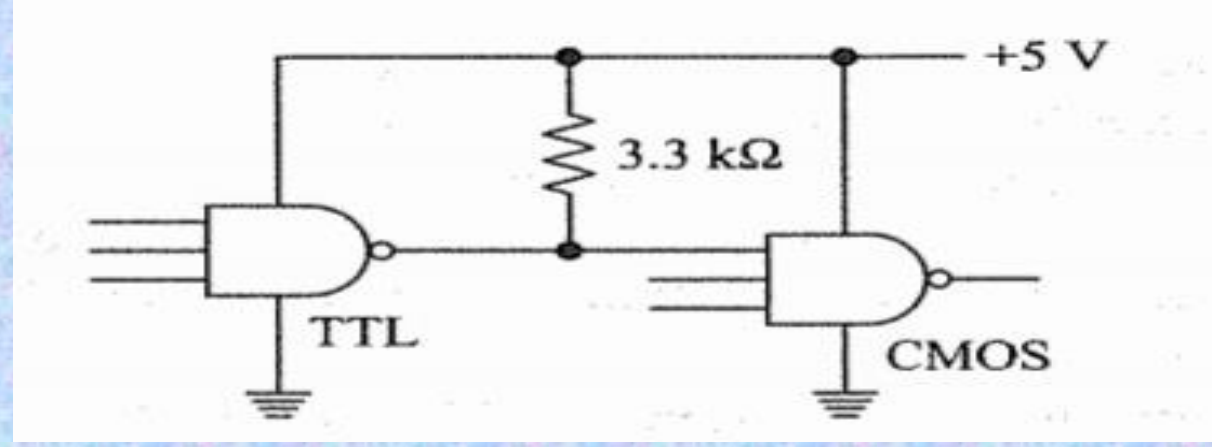



Fig. 1.35 TLL driver and CMOS load

- The gate capacitance of the CMOS load has to be charged through the pull-up resistor. This slows down the switching action. If speed is important, you can decrease the pull-up resistance. The minimum resistance is determined by the maximum sink current of the TTL device: $I_{OL,max} = 16$ mA. In the worst case the supply voltage may be as high as 5.25 V, so the minimum resistance is

# Digital Electronic

$$R_{\text{min}} = \frac{5.25\ \text{V}}{16\ \text{mA}} = 328\ \Omega$$

- The nearest standard value is 330 Ω, which you should consider the absolute minimum value for the pull-up resistor. And you would use this only if switching speed were critical. In many applications, a pull-up resistance of 3.3 kΩ is fine.

# Digital Electronic

- Incidentally, the other inputs of the TTL driver and CMOS load (Fig. 1.35) are connected to signal lines not shown. Also, the use of 3-input gates is arbitrary. You can interface gates with any number of inputs. If more than one TTL chip is being interfaced to the CMOS load, connect each TTL driver to a separate pull-up resistor and CMOS input.

# Digital Electronic

**Different Supply Voltages**

- CMOS performance deteriorates at lower voltages because the propagation delay time increases and the noise immunity decreases. Therefore, it is better to run CMOS devices with a supply voltage between 9 and 12 V. One way to use a higher supply voltage is with an open-collector TTL driver (Fig. 1.36). Recall that the output stage of an open collector TTL device consists only of a sink transistor with a floating collector. In Fig. 1.36. this open collector is connected to a supply voltage of +12 V through a pull-up resistance of 6.8 kΩ. Likewise, the CMOS device now has a supply voltage of +12 V.

# Digital Electronic

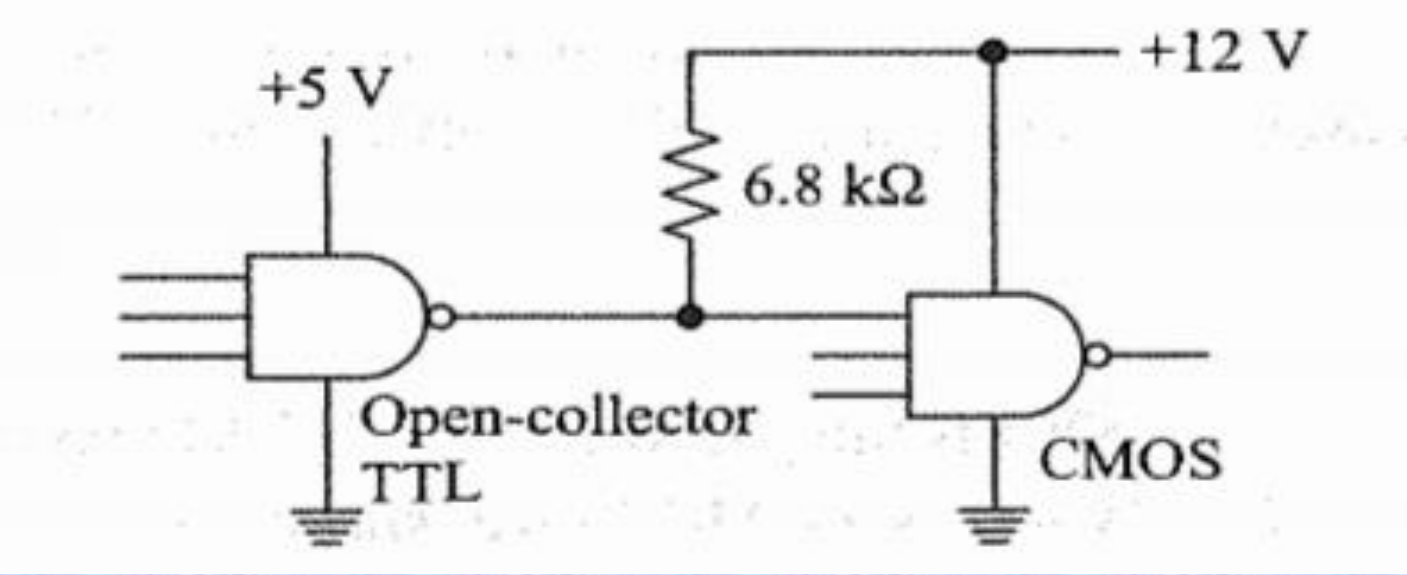



Fig. 1.36 Open-collector TTL driver allows higher CMOS supply voltage

# Digital Electronic

- When the TTL output is low, we can visualize a ground on the lower end of the pull-up resistor. Therefore, the TTL device has to sink approximately

$$I_{sink} = \frac{12\ V}{6.8\ k\Omega} = 1.76\ mA$$

- When the TTL output is high, the open-collector output rises passively to +12 V. In either case, the TTL outputs are compatible with the CMOS input states.

# Digital Electronic

- The passive pull-up in Fig. 1.36 produces slower switching action than before. For instance, with a gate input capacitance of I0 pF, the pull-up time constant is

  RC=(6.8 kΩ)(10pF)= 68 ns

- If this is a problem, reduce the pull-up resistance to its minimum allowable value of

$$R_{min} = \frac{12\ \text{V}}{16\ \text{mA}} = 750\ \Omega$$

# Digital Electronic

- Then the pull-up time constant decreases to

$$RC = (750\ k\Omega)\ (10\ pF) = 7.5\ ns$$

**CMOS level Shifter**

- Figure 1.37 shows a 40109, called a level shifter. The input stage of the chip uses a sup-ply voltage of +5 V, while the output stage uses + 12 V. In other words, the input stage interfaces with TTL, and the output stage interfaces with CMOS.

# Digital Electronic

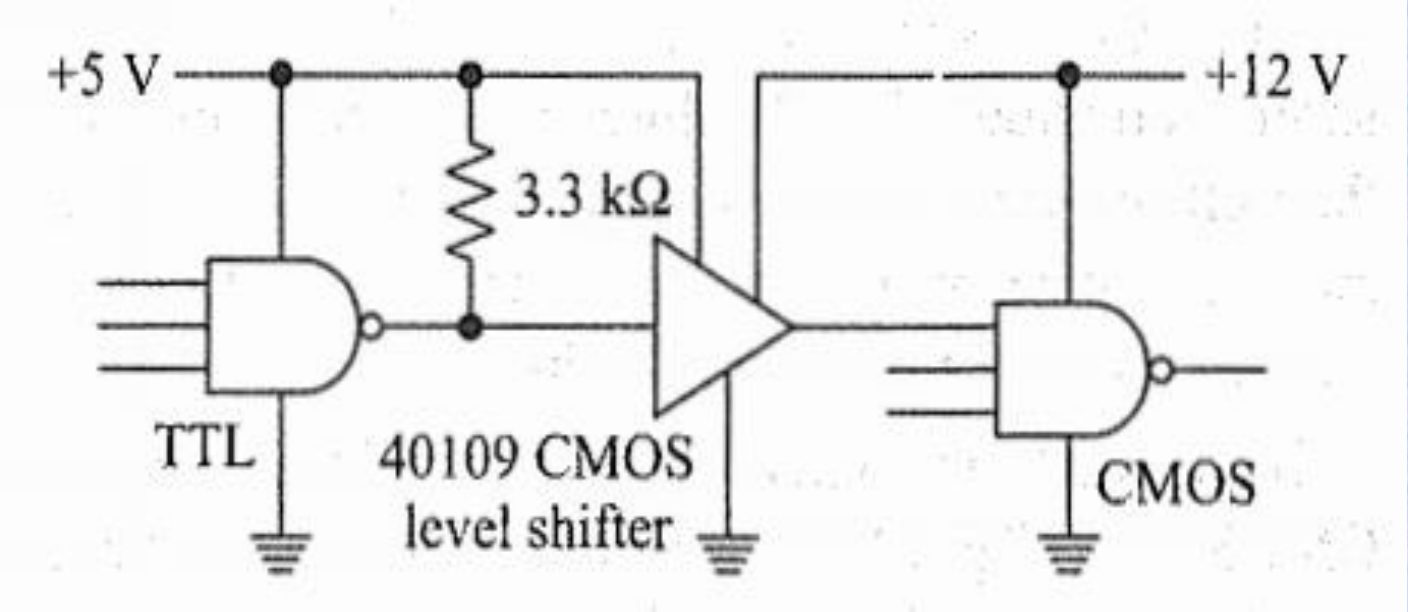



Fig. 1.37 CMOS level shifter allows the use of 5-V and 12-V supplies

# Digital Electronic

- In Fig. 1.37, a standard TTL device drives the level shifter. This produces active TTL pull-up to at least +2.4 V. Beyond this level, the pull-up resistor takes over and raises the voltage to +5 V, which ensures a valid high-state input to the level shifter. The output side of the level shifter connects to+12V (this can be changed to any voltage from 3 to 15 V). Since the CMOS load runs off of+12 V, it has better propagation delay time and noise immunity.
- In summary, TTL has to run off of +5 V, but CMOS does better with a supply voltage of +12 V. This is the reason for using a level shifter between the TTL driver and the CMOS load.

# Digital Electronic

## 1.7 CMOS-TO-TTL INTERFACE

- In this section, we discuss methods for interfacing CMOS devices to TTL devices, Again, the problem is to shift voltage levels until the CMOS output states fall inside the TTL input windows. Specifically, we have to make sure that the CMOS low-state output is always less than 0.8 V, the maximum allowable TTL low-state input voltage. Also, the CMOS high-state output must always be greater than 2 V, the minimum allowable TTL high-state input voltage.

# Digital Electronic

**Supply Voltage at 5 V**

- One approach is to use +5 V as the supply voltage for the driver and the load, as shown in Fig. 1.38. A direct interface like this forces you to use a low- power Schottky TTL load (or two low-power TTL loads). Why? Because a low-power Schottky device has these worst-case input currents:

$$I_{IL,\max} = -360\ \mu\text{A} \quad I_{IH,\max} = 20\ \mu\text{A}$$

# Digital Electronic

- Data sheets for 74C00 devices list these worst- case output currents for CMOS driving TTL:

$$I_{OL,\max} = 360\ \mu A \quad I_{OH,\max} = -360\ \mu A$$

- This tells us that a CMOS drive can sink 360 µA in the low state, exactly the input current for a low-power Schottky TTL devices. On the other hand, the CMOS driver can source 360 µA, which is more than enough to handle the high-state input current (only 20 µA). So the sink current limits the CMOS/74LS fanout to 1.

# Digital Electronic

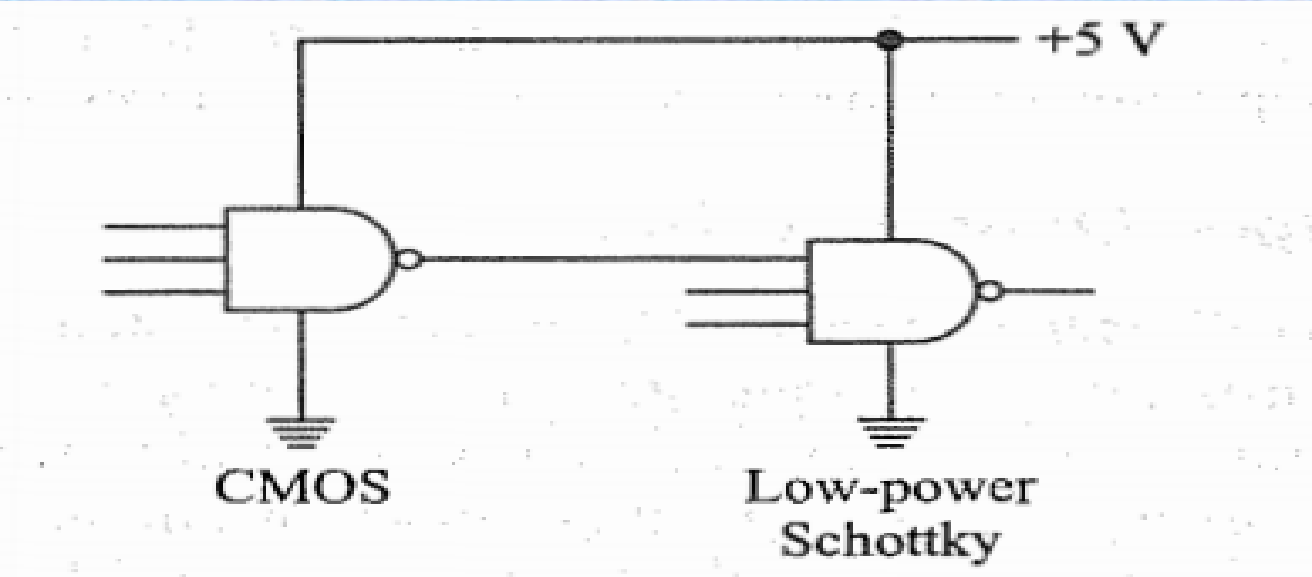



Fig. 1.38 CMOS driver and low-power Schottky TTL load

# Digital Electronic

- CMOS can also drive low-power TTL devices. The limiting factor again is the sink current. Low-power TTL has a worst-case low-state input current of 180 μA. Since a CMOS driver can sink 360 μA, it can drive two low-power TTL devices. Briefly stated, the CMOS/74L fanout is 2.
- CMOS cannot drive standard TTL directly because the latter requires a low-state input current of -1.6 mA, for too much current for a CMOS device to sink without entering the TTL indeterminate region. The problem is that the sink transistor of a CMOS device is equivalent to a resistance of approximately 1.11 kΩ (worst case). The CMOS output voltage equals the product of 1.6 mA and 1.11 kΩ, which is 1. 78 V. This is too large to be low-state TTL input.

# Digital Electronic

## Using a CMOS Buffer

- Figure 1.39 shows how to get around the fanout limitation just discussed. The CMOS driver now connects directly to a CMOS buffer, a chip with larger output currents. For instance, a 74C902 is a hex buffer, or six CMOS buffers in a single package. Each buffer has these worst-case output currents:

$$I_{OL,\max} = 3.6\ \text{mA} \quad I_{OH,\max} = 800\ \mu\text{A}$$

# Digital Electronic

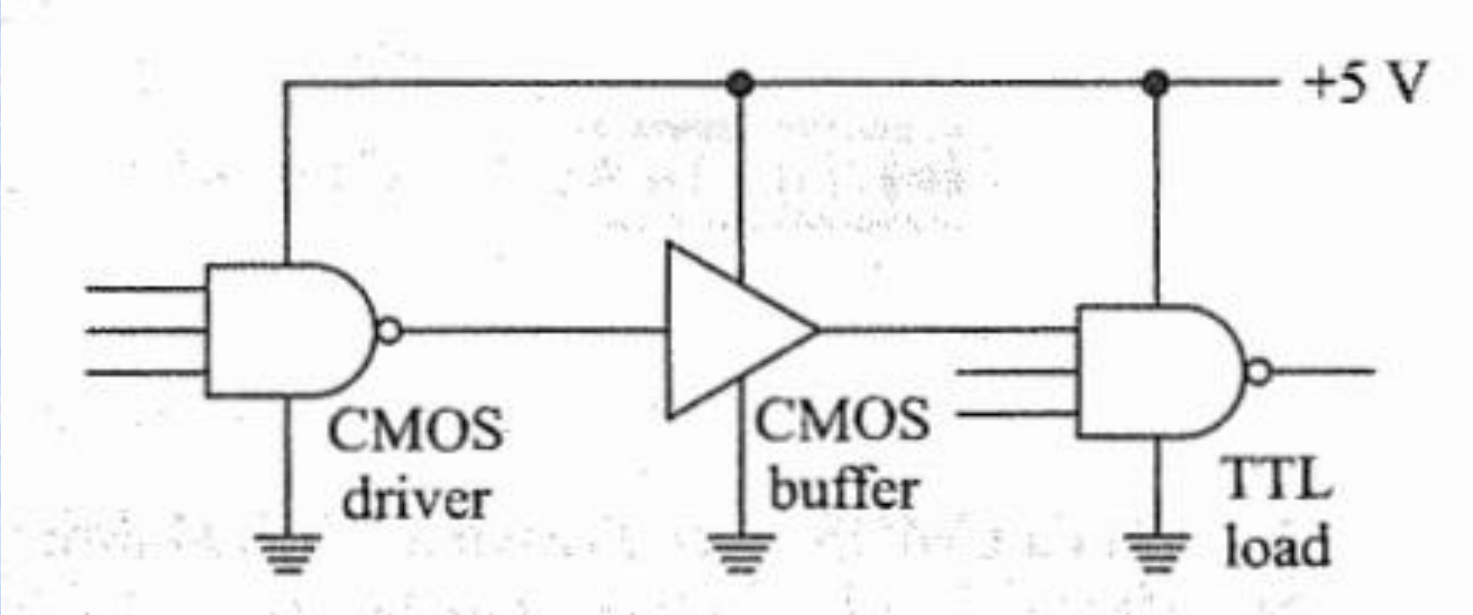



Fig 1.39 CMOS buffer can drive standard TTL load

# Digital Electronic

- Since a standard TTL load has a low-state input current of 1.6 mA and a high-state input current of 40 μA, a 74C902 can drive two standard TTL loads. If you use one-sixth of a 74C902 in Fig. 1.39, the CMOS/TTL fanout is 2. Other available buffers are the CD4049A (inverting), CD4050A (noninverting), 74C901 (inverting), etc.

# Digital Electronic

**Different Supply Voltages**

- CMOS buffers like the 74C902 can use a supply voltage of 3 to 15V and an input voltage of -0.3 to 15 V. The input voltage can be greater than the supply voltage without damaging the device. For instance, you can use a high-state input of +12 V even though the supply voltage is only +5 V.
- Figure 1.40 shows how to use the previous idea to our advantage. Here, the supply pin of the CMOS driver is connected to + 12 V. On the other hand, the supply pin of the CMOS buffer is connected to +5 V to produce the TTL interface. Therefore, the input to the CMOS buffer will be as much as +12 V, even if its supply voltage is only +5 V. The fanout of this interface is still **two** standard TTL loads.

# Digital Electronic

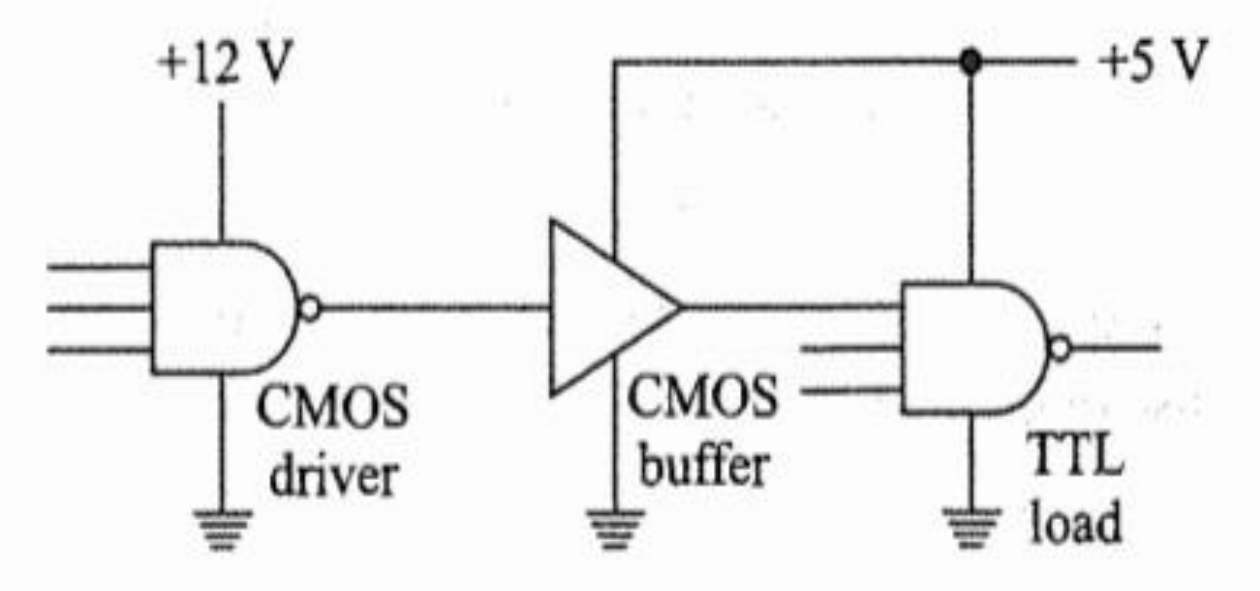



Fig. 1.40 CMOS driver runs better with 12-V supply

# Digital Electronic

## Open-Drain Interface

- Recall open-collector TTL devices. The output stage consists of a sink transistor with a floating collector. Similar devices exist in the CMOS family. Known as open-drain devices, these have an output stage consisting only of a sink MOSFET. An example is the 74C906, a hex open-drain buffer.

# Digital Electronic

- Figure 1.41 shows how an open-drain CMOS buffer can be used as an interface between a CMOS driver and a TTL load. The supply voltage for most of the buffer is +12 V. The open drain, however, is connected to a supply voltage of +5 V through a pull-up resistance of 3.3 kΩ. This has the advantage that both the CMOS driver and the CMOS buffer run off of +12 V, except for the open-drain output which provides the TTL interface.

# Digital Electronic

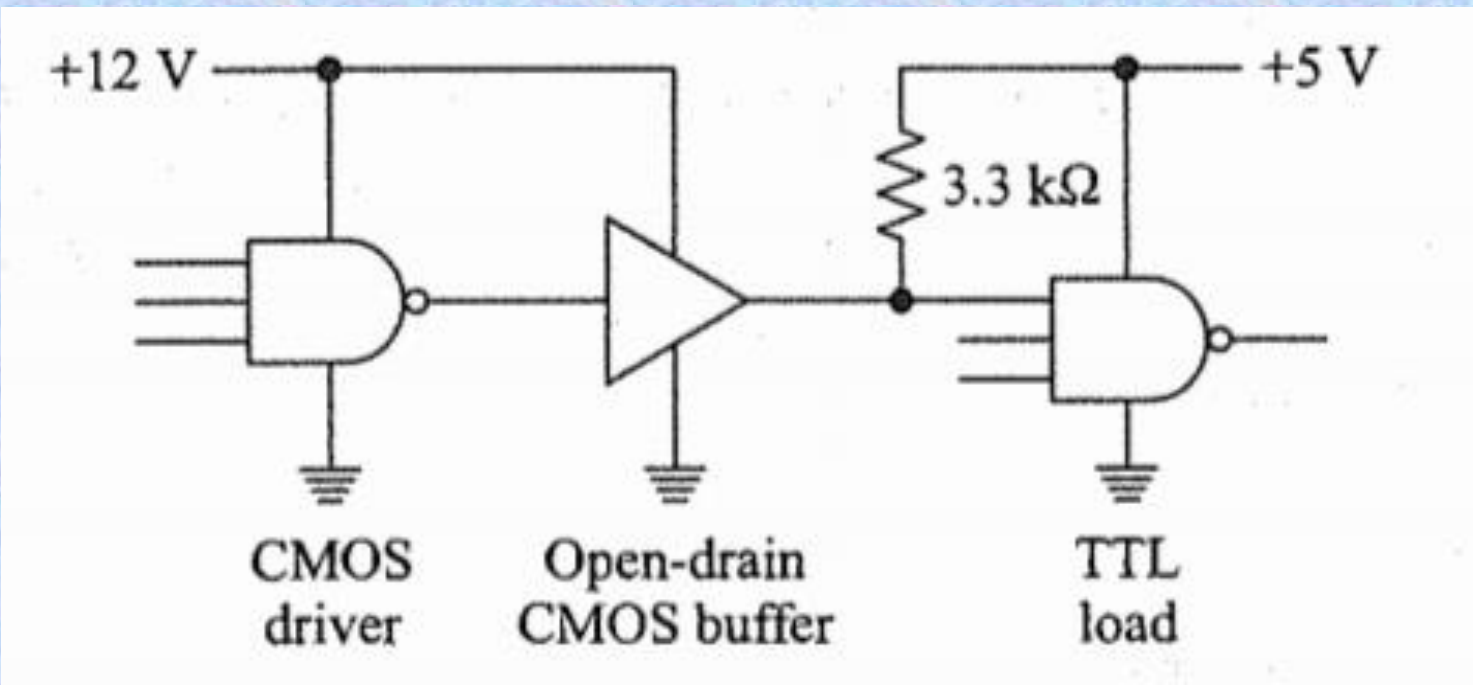



Fig. 1.41 Open-drain CMOS buffer increases sink current