

Lecture 1

1. Digital Computers:

The characteristic of digital systems is its manipulation of discrete elements of information. Examples of discrete elements may be electrical impulses, decimal digits, the letters of the alphabet, arithmetic operations, punctuation marks, and any other meaningful symbols. Discrete elements of information are represented in a digital system by physical quantities called signals. Electrical signals such as voltages are the most common. The signals in all present-day electronic digital systems have only two discrete values and are said to be binary.

2. Number Systems (Binary, Octal , Decimal and Hexadecimal):



Example: $(7392.54)_{10} = 10^{3*7} + 10^{2*3} + 10^{1*9} + 10^{0*2} + 10^{-1*5} + 10^{-2*4}$ =7000+300+20+9+0.5+0.04

• When the **base** is equal to 10 the numbering system is named **Decimal** and the **coefficients range** is (0,1,2,3,4,5,6,7,8,9)

In general a number with decimal points is represented by a series of coefficients as follows:

 $(a_n...a_3 a_2 a_1 a_0 \cdot a_{-1} a_{-2} a_{-3}...a_{-m})_{10}$ The a_j coefficients are one of the digits (0, 1, 2, 3..., 9) $a_3*10^3_+ a_2*10^2_+ a_1*10^1_+ a_0*10^0_+ a_{-1}*10^{-1}_+ a_{-2}*10^{-2}_+ a_{-3}*10^{-3}$

• The **Binary** number system is a different number system, the **coefficients** are (**0** and **1**) only and the **base** or radix **2**, Ex:



• When the **base** is equal to 8 the numbering system is named **Octal** and the **coefficients** range is (0, 1, 2, 3, 4, 5, 6, 7), Ex:



When the base is equal to 16 the numbering system is named Hexadecimal and the coefficients range is (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F), where A=10, B=11, C=12, D=13, E=14, F=15. Ex :



In general a number expressed in base (r) system has coefficients (0, 1...r-1), multiplied by power of r

 r^{n} r^{3} r^{2} r^{1} r^{0} r^{-1} r^{-2} $r^{-m} \longrightarrow Weights$ (a_{n} a_{3} a_{2} a_{1} a_{0} . a_{-1} a_{-2} a_{-m}) $r \longrightarrow Base$

 $r^{n}*a_{n}+\ldots\ldots+r^{3}*a_{3}+r^{2}*a_{2}+r^{1}*a_{1}+r^{0}*a_{0}+r^{-1}*a_{-1}+r^{-2}*a_{-2}+\ldots\ldots r^{-m}*a_{-m}$

When the base of the number is less than (10) the needed (r) digit of the coefficients are borrowed from the decimal system. If the base is greater than (10) then the letters of the alphabet are used.

3. Conversion from Decimal to Other Bases and vice versa.

3. A The conversion from any base r to decimal:

A number expressed in base r can be converted to its decimal equivalent by multiplying each coefficient with corresponding power of r and adding.

Ex:

$$7^{2}$$
 7^{1} 7^{0} 7^{-1}
(6 3 0 . 4)₇ =6*7²+3*7¹+0*7⁰+4*7⁻¹
= 49*6+21+0+4/7= 294+21+0+0.571=(315.571)_{10}

$$8^{2} 8^{1} 8^{0} 8^{-1}$$
(6 3 0 . 4)₈ =6*8²+3*8¹+0*8⁰+4*8⁻¹
= 64*6+24+0+4/8= 384+24+0+0.5=(408.5)₁₀
2^{3} 2² 2¹ 2⁰ 2⁻¹ 2⁻² 2⁻³
(1 1 1 0 . 1 0 1)₂ =1*2³+1*2²+1*2¹+0*2⁰+1*2⁻¹+0*2⁻²+1*2⁻³
=8+4+2+0+1/2+0+1/8=14+0.5+0+0.125
=(14.625)₁₀
16² 16¹ 16⁰ 16⁻¹
(F 3 A . B)₁₆ =F*16²+3*16¹+A*16⁰+B*16⁻¹
= 15*16²+3*16¹+10*16⁰+11*16⁻¹
=15*256+3*16+10*1+11/16
=3840+48+10+0.6875=(3898.6875)₁₀

3. B The Conversion from decimal to any base r:

Note: The conversion is more convenient if the number is separated into an integer part and a fraction part so the conversion of each part is done separately. Ex: Convert the decimal number (14.625) to binary (base 2)

Integer	Remainder	
14÷2		
7÷2	0	a_0
3÷2	1	a_1
1÷2	1	a_2
0	1	a3

 $(14)_{10} = (1110)_2$

	Integer	Fraction	
		0.625 * 2	=1.25
a-1	1	0.25 *2	=0.5
a -2	0	0.5 *2	=1.0
a-3	1	0.00	

 $(0.625)_{10} = (0.101)_2$ (14. 625)_{10} = (1110.101)_2 Ex: Convert the decimal number (315.571) to (base 7)

Integer	Remainder	
315÷7		
45÷7	0	a_0
6÷7	3	a_1
0	6	a_2

 $(315)_{10} = (630)_7$

	Integer	Fraction	
		0. 571 * 7	=3. 997
a-1	3	0.997 *7	=6. 979
a-2	6	0.979 *7	=6.853
a-3	6	0.853	

 $(0.571)_{10} = (0.366)_7$ $(315.571)_{10} = (630.366)_7$

Ex: Convert the decimal number (314.21) to Hexadecimal (base 16)

Integer	Remainder	
314÷16		
19÷16	Α	a_0
1÷16	3	a_1
0	1	a_2

(314)₁₀=(13A)₁₆

	Integer	Fraction	
		0. 21	-3 36
		* 16	-5.50
a-1	3	0.36	-5 76
	5	*16	-5.70
a-2	5	0.76	-12 16
	5	*16	-12.10
a-3	C	0.16	
	C		

 $(0. 21)_{10} = (0.35C)_{16}$ $(314.21)_{10} = (13A .35C)_{16}$

HW. Convert the following number to the indicated bases

- 1. (214.3)₁₀ to base 4.
- 2. (10101.101)₂ to decimal.
- 3. (124.03)₅ to base 7.

- 4. (346.67)₁₀ to base 16.
- 5. (124.34)₁₀ to base 12.
- 6. (110101.1101)₂ to decimal.
- 7. $(42F.CB)_{16}$ to decimal
- 8. (111011010.001101)₂ to Octal.
- 9. (12A.8)₁₂ to Decimal.

4. A number with different bases:

Dec	imal		Binary				Oc	tal	Hexadecimal	
(0,1	,,9)			(0,1)			(0,1	,7)	(0,1,9),AF)
10 ¹	100	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	8^{1}	8^{0}	16 ¹	16^{0}
10	1	16	8	4	2	1	8	1	16	1
	0					0		0		0
	1					1		1		1
	2				1	0		2		2
	3				1	1		3		3
	4			1	0	0		4		4
	5			1	0	1		5		5
	6			1	1	0		6		6
	7			1	1	1		7		7
	8		1	0	0	0	1	0		8
	9		1	0	0	1	1	1		9
1	0		1	0	1	0	1	2		А
1	1		1	0	1	1	1	3		В
1	2		1	1	0	0	1	4		С
1	3		1	1	0	1	1	5		D
1	4		1	1	1	0	1	6		Е
1	5		1	1	1	1	1	7		F
1	6	1	0	0	0	0	2	0	1	0
1	7	1	0	0	0	1	2	1	1	1
1	8	1	0	0	1	0	2	2	1	2
1	9	1	0	0	1	1	2	3	1	3
2	0	1	0	1	0	0	2	4	1	4
2	1	1	0	1	0	1	2	5	1	5
2	2	1	0	1	1	0	2	6	1	6
2	3	1	0	1	1	1	2	7	1	7
2	4	1	1	0	0	0	3	0	1	8
2	5	1	1	0	0	1	3	1	1	9

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5. Octal, Hexadecimal and Binary numbers:

The conversion from and to binary (base 2), Octal (base 8) and hexadecimal (base 16) plays an important part in digital computers, since $2^3=8$ and $2^4=16$ each octal digit corresponds to 3-binary digits and each hexadecimal digit corresponds to 4-binary digits.

Ex:(1) (10110001101011.11110000011)2=(?)₈=(26153.7406)₈

		$=(?)_{16}=(2C0B.F00)_{16}$							
(0 10	110	001	101	011	•	111	100	000	11 0)2
(2	6	1	5	3	•	7	4	0	6)8

(00 10	1100	0110	1011	•	1111	0000	011 0) ₂
(2	С	6	В	•	F	0	6)16

(2) $(673.124)_8 = (?)_2 = (110111011.0010101)_2$

(6	7	3	•	1	2	4)8
(110	111	011	•	001	010	100)2

$(3) \qquad (306.D)_{16} = (?)_2 = (1100000110.1101)_2$

(3	0	6	•	D) ₁₆
(0011	0000	0110	•	1101)2

HW. Convert the following number to the indicated bases

- 1. $(456.7)_8$ to hexadecimal using the binary as intermediate base.
- 2. (98FE.0AB)₁₆ to Octal using the binary as intermediate base.
- 3. $(10AB.FE)_{16}$ to octal using the binary as intermediate base.
- 4. (6754.231)₈ to Hexadecimal using the binary as intermediate base
- 5. (111011010.001101)₂ to Octal.
- 6. (AD09.3C)₁₆ to Binary.

6. Arithmetic Operation:

Addition (+), Subtraction (-), Multiplication (*)							
Carry		(1)	(1)	(1)	(1)		
Augend	(1	0	1	1	0	1)2	
Addend	(1	0	0	1	1	1)2	+
Sum	(10	1	0	1	0	0)2	
			1	0			
Borrow			0 -	σ1	0		
Minuend	(1	0 ·	1 -	1 1	or 1)2	
Subtrahend	(1	0	0	1	1 1)2 -	
Difference	(0	0	0	1	1 0)2	
Multiplicand		(1	0	1	1)2	
Multiplier		(1	0	$1)_{2}$	*
-		(1)	1	0	1	1	
		0	0	0	0		+
	1	0	1	1			
Product	(1	1	0	1	1	1)2	

HW. Perform the following operation without converting to decimal or any other base:

- 1. (1101.01 * 10.1)₂=
- 2. (D39 + 16A)₁₆=
- 3. (243.13 144.02)₅ =
- 4. $(11100.01 1110.11)_2 =$
- 5. (243 * 24)5=
- 6. (FB09 ED32)₁₆=
- 7. (227.65 + 624.31)8=
- 8. (FD0D AE21)₁₆ =
- 9. (323 * 32)₄ =

7. Complement and Subtraction using 1's and 2's Complement.

7.1 Complement:

Complements are used in digital computers for simplifying the subtraction operation and for logical manipulation. There are two types of complements for each base (r) system:

I. The r's complements

II. The (r-1)'s complements

7.1.1 The r's complements: A positive number **N** in base **r** with an integer part of **n** digits, the r's complement of **N** is defining as follows:

for N≠0
for N=0

Ex:

(1) The 10's complement of $(925.67)_{10}$ is N=925.67, r=10, n=3 \rightarrow the 10's complement equal to: $(10^3-925.67)_{10}=1000-925.67=(74.33)_{10}$

	9	9	9		9			
0	Ю	10	10		10	10		
(1	Ø	Ð	Ø		-0	Ø)10	-
(9	2	5		6	7)10	
(0	0	7	4	•	3	3)10	

(2) The 10' complement of $(0.3267)_{10}$ is N=0.3267, r=10, n=0→the 10's complement equal to: $(10^{0}-0.3267)_{10}=1-0.3267=(0.6733)_{10}$

		9	9	9		
0		10	10	10	10	
(1	•	Ø	Ø	Ø	10) ₁₀	-
(0	•	3	2	6	7)10	
(0	•	6	7	3	3)10	

(3) The 2's complement of $(101100)_2$ is N=101100, r=2, n=6 \rightarrow the 2's complement equal to : $(2^6)_{10}$ - $(101100)_2$ = $(100000-101100)_2$ = $(10100)_2$

	1	1	1				
0	10	10	10	10			
(†	-0	Ø	Ø	Ø	0	0)2	-
(1	0	1	1	0	0)2	
(0	0	1	0	1	0	0)2	

(4) The 2's complement of $(0.0110)_2$ is N=0.0110, r=2, n=0 \rightarrow the 2's complement equal to : $(2^0)_{10}-(0.0110)_2=(1-0.0110)_2=(0.1010)_2$

		1	1			
0	•	10	10	10		
(†	•	Ø	Ø	Ø	0)2	-
(0	1	1	0)2	
(0	•	1	0	1	0)2	

(5) The 9'complement of $(0.3267)_{10}$ is N=0.3267, r=10, n=0,m=4 \rightarrow the 9's complement equal to: $(10^0-10^{-4}-0.3267)_{10}=(1-0.0001)-0.3267=$

 $=0.9999-0.3267=(0.6732)_{10}$

		~	~				
		9	9	9)		
0		10	10	1	Ø	10	
(ł	•	O	Ø	C	٢	10) ₁₀	-
(0	•	0	0	0)	1)10	
(0	•	9	9	9)	9)10	
	(0	•	9	9	9	9)10	
	(0	•	3	2	6	7)10	
	(0	•	6	7	3	2)10	

7.1.2 The (r-1)'s complements:

A positive number N in base \mathbf{r} with an integer part of \mathbf{n} digits and a fraction part of \mathbf{m} digits, the (r-1)'s complement of N is defined as follows:



(1) The 9's complement of $(925.67)_{10}$ is N=925.67, r=10, n=3, m=2 \rightarrow the 9's complement equal to: $(10^3 - 10^{-2} - 925.67)_{10} = (1000 - 0.01) - 925.67 = 999.99 - 925.67 = (74.32)_{10}$

	9	9	9		9			
0	10	10	10		1	0	10	
(1	Ø	Ø	Ø	•	0	٢	10)10	-
(0		0		1)10	
(0	9	9	9	•	9		9) ₁₀	
	(9	9	9		9	9) ₁₀	
	(9	2	5		6	7)10	-
	(0	7	4		3	$2)_{10}$	

(2) The 9'complement of $(0.3267)_{10}$ is N=0.3267, r=10, n=0,m=4 \rightarrow the 9's complement equal to: $(10^{0}-10^{-4}-0.3267)_{10}=(1-0.0001)-0.3267=$

 $=0.9999-0.3267=(0.6732)_{10}$

		9	9	9)		
0		10	10	1	TŪ	10	
(ł	•	Ø	Ø	e	5	10) ₁₀	-
(0	•	0	0	0)	1)10	
(0	•	9	9	9)	9)10	
	(0	•	9	9	9	9)10	-
	(0	•	3	2	6	7)10	
	(0	•	6	7	3	2)10	

(3) The 1's complement of $(101100)_2$ is N=101100, r=2, n=6 ,m=0→the 1's complement equal to: $(2^6-2^0)_{10}-(101100)_2=(1000000-1)_2-(101100)_2$

 $=(1111111-101100)_2=(10011)_2$

0 (†	1 10 -0	1 10 0	1 10 0	1 14 0	1 + -1 0	0	1 10 0)2	-
()	1	1	1	1	1		$\frac{1}{2}$ 1) ₂	
		(1) (1) (0)	1 0 1	1 1 0	1 1 0	1 0 1	$ \begin{array}{r} 1)_2 \\ 0)_2 \\ 1)_2 \end{array} $	-

(4) The 1's complement of $(0.0110)_2$ is N=0.0110, r=2, n=0 ,m=4 \rightarrow the 1's complement equal to: $(2^0-2^{-4})_{10}-(0.0110)_2=(1-0.0001)_2-(0.0110)_2$

 $=(0.1111-0.0110)2=(0.1001)_2$

0 (†	•	1 10 10	1 10 67	1 10 O	10 10)2	_
(•	U	U	U	$(1)_{2}^{2}$	_
(0	•	1	1	1	1)2	
	(0).	1	1 1	1)2	-
	(().	0	1 1	0)2	
	(().	1	0 () 1)2	

(5) The 15's complement of (E58C.D)₁₆ is N= E58C.D, r=16, n=4 m=1 \rightarrow the 16's complement equal to : (16⁴-16⁻¹)₁₀-(E58C.D)₁₆=(10000-0.1)₁₆- (E58C.D)₁₆ =(1A73.2)₁₆

0 († (F 10 10	F H O] 7 = -{	F HØ)	F 10 0	•	10 & 1)16)16	-
(F	F]	F	F		F)16	
	((F E 1	F 5 A	F 8 7	F C 3	•	F D 2)16)16)16	-

Note:

1. The 9's complement of a decimal number is formed simply by subtracting every digit from 9.

2. The 1's complement of a binary number is even simpler to form: 1's are changed to 0's and 0's to 1's.

3. The r's complement can be obtained from the (r-1)'s complement after the addition of r^{-m} to the least significant digit.

Ex: the 2's complement of $(10110100)_2$ obtained from the 1's complement as follows: 1's complement of $(10110100)_2=(2^5-2^{-0})_{10}-(10110)_2=(100000-1-10110)_2=$

2's complement=1's complement + r^{-m} =1001+1=(1010)₂

2's complement directly= $(2^5)_{10}$ -(10110)₂=(100000-10110)= (1010)₂

	1	1	1			
0	10	Ю	10	10		
(†	-0	Ø	Ø	Ø	0)2	-
(1	0	1	1	0)2	
(0	0	1	0	1	0)2	

5.1.2 The complement of the complement is restoring the number its original value. Ex: the r's complement of N is r^n -N

The r's complement of (r^n-N) is $r^n-(r^n-N)=r^{n'}-r^n+N=N$

H.W Prove the above example using (r-1)'s complement.

8. Alphanumeric Codes:

Many applications of digital computers require handling name as well as letters. An alphanumeric code is a binary code of a group of elements consisting of 10 decimal digits, the 26 letter of alphabet, certain number of special symbols such as , , ... etc. The total number of elements in an alphanumeric group is >36. So it must be coded with minimum number of bits $(2^{6}=64)$.

• ASCII code (American Standard Code for Information Interchange) 7-bit Length code.

Letters	ASC	CII code	Letters	ASC	II code
	decimal	binary		decimal	binary
А	65	100 0001	а	97	110 0001
В	66	100 0010	b	98	110 0010
:					
Z	90	101 1010	Z	122	111 1010
0	48	011 0000			
1	49	011 0001			
:					
9	57	011 1001			
\$	36	010 0100			
(40	010 1000			
?	47	010 1111			

• EBCDIC code (Extended **BCD** Interchange Code) 8-bit Length code.

Lecture 2

9. Binary Logic and Gates

7.1 Binary logic:

Binary logic deals with the variables take two discrete values true and false, yes and no. Binary logic is used to describe, in a mathematical way, the manipulation and processing of binary information. It particularly suited for analysis and design of digital systems. Binary Logic is equivalent to Boolean algebra.

7.2 Definition of Binary logic:

Binary logic consists of binary variables and logic operation. The variables are designated by letters e.g. A, B, C, r, w, x, y with only two distinct values: 1 and 0. The basic logical operators are AND, OR and NOT.

AND	similar to * in binary arithmetic			
OR	similar to + in binary arithmetic	but	1 + 1 = 10	(in binary
				arithmetic)
			1 + 1 = 1	(in binary logic)



Timing diagram illustrate the response of each circuit to each of 4 input binary combinations (00,01,10,11)

7.3 Logic Gates:

Digital Circuits, Switching Circuits, Logic Circuits and Logic Gates are the same. Gates are block of hardware that produces a logic-1 or logic-0 output signal if input logic requirement are satisfied.



The mathematical system of binary logic is better known as Boolean or switching algebra. This algebra is conveniently used to describe the operation of complex network of digital circuits. Designers of digital systems use Boolean algebra to transform circuits diagram to algebraic expression and vice versa.

10.Integrated Circuits:

Is a small silicon semiconductor crystal, called a chip, containing electrical components such as transistor, diodes, resistor and capacitor. The various components are interconnected inside the chip to form electronic circuits. The chip is mounted on a metal or plastic packaged, and connection are welded to external pins to form the IC. IC's come in two types: 1) Flat package 2) dual package

As the technology of ICs has improved, number of gates that can be put on a single silicon chip has increased considerably.

- SSI chip contains less than 10 gates.
- MSI chip contains between 10 to 100 gates.
- LSI chip contains between 100 to 1000 gates.
- VLSI chip contains between thousands of gates.

	a	b	
1	X+0=X	X.1=X	Identity Element
2	X+1=1	X.0=0	
3	X+X=X	X.X=X	
4 $\forall X \in B \exists \overline{X} s.t$	$X + \overline{X} = 1$	X.X=0	Complement Definition
5	$\overline{\overline{X}}=X$		
6	X+Y=Y+X	X.Y=Y.X	Commutative Law
7	X+(Y+Z)=(X+Y)+Z	X.(YZ)=(XY).Z	Associative Law
8	X.(Y+Z)=(X.Y)+(X.Z)	X+(Y.Z)=(X+Y).(X+Z)	Distributive Law
9	$\overline{(X+Y)} = \overline{X}.\overline{Y}$	$\overline{(X.Y)} = \overline{X} + \overline{Y}$	Demorgan's Theorem
10	X+XY=X	X(X+Y)=X	Absorption Theorem

11.Basic Identity of Boolean Algebra:

12.Boolean Functions:

Boolean functions are formed from binary variables, logic operators and equal sign. the function value can be either 1 or 0:

Ex: $F1 = xy\overline{z}$ $F2 = x + \overline{y}z$

OR and NOT get.

A Boolean function also represented in truth table. A Boolean function may be transformed from an algebraic expression into a logic diagram or circuit composed of AND,

NOTE: The operator precedence for evaluating Boolean expression is:

1. Parentheses 2. NOT 3. AND 4. OR Boolean Expression

 Image: Description of the second seco

Boolean Logic Circuit Truth Table (T.T.) Expression $F1 = xy\bar{z}$ F1 = x y zTruth Table of F1 х z' F1=xyz' y y Z Х 0 0 0 1 0 Z 0 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 0 1 1 0

	1 1 1	0 1 1	1 0 1	0 1 0		0 1 0
F2 = $x + \overline{y}z$ x y z F2=x+y z F2=x+y z	x 0 0 0 1 1 1 1 1	T1 y 0 1 1 0 0 1 1 1	ruth z 0 1 0 1 0 1 0 1 0 1	Tab y' 1 1 0 0 1 1 0 0 0	ble of y'z 0 1 0 0 0 1 0 0 0	F2 x+y'z 0 1 0 0 1 1 1 1 1 1

Complement of a function:

The complement of any function F is F or \overline{F} its value can be obtained by interchange the (1's to 0's) and (0's to 1's) in the value of F. the complement of a function may be obtained algebraically through Demerger's theory.

Ex: Fined \overline{F} of F1 and F2.

$$\overline{F1} = \overline{(xy\overline{z})} = \overline{x} + \overline{y} + \overline{\overline{z}} = \overline{x} + \overline{y} + z$$
$$\overline{F2} = \overline{(x + \overline{y}z)} = \overline{x}. \ \overline{\overline{y}z} = \overline{x}. \ (\overline{\overline{y}} + \overline{z}) = \overline{x}. \ (y + \overline{z})$$

Lecture 3

13.Simplification of Boolean Functions using Boolean algebra.

<u>Literal</u>: is a single variable within the term that may be complemented or not. When a Boolean function is implemented with logic gates, each literal in Boolean function is designated an input to gate and each terms is implemented with gate. The minimization of a number of literal and the number of terms results in circuit with less equipment. Boolean algebra is a useful tool for simplifying digital circuit. Functions below simplified by using Boolean algebra.

Reduce the following Boolean expression using Boolean algebra to the indicated number of literals:

1)	F1=x'yz+x'yz'+xy	to one literal
	$= \underline{x'yz} + \underline{x'yz'} + xy$	
	=x'y(z+z')+xy	(Distributive law)
	=x'y.1+xy	(Complement definition)
	=x'y+xy	(Identity element)

- =y(x'+x) (Distributive law) =y.1 (Complement definition) F1=y (Identity element)
- 2) F2=x+(x'y) to two literals =(x+x')(x+y) (Distributive law) =1.(x+y) (Complement definition) F2=x+y (Identity element).
- 3) F3=xy+x'z+yz to four literals = xy+x'z+yz.1 (Iidentity element) = xy+x'z+yz(x+x') (Complement definition) = xy+x'z+xyz+x'yz (Distributive law) =xy(1+z)+x'z(1+y) (Distributive law) =xy.1+x'z.1 (x+1)=1 F3=xy+x'z (Iidentity element)



HW.

Q1) Represent the decimal number (1729) using the following codes:

1)BCD 2)Excess-3

3)(8,4,-2,-1) 4) (2,4,2,1) self-complemented

Q2) Reduce the following Boolean expression using Boolean algebra to the indicated number of literals:

1. $XYZ + \overline{X}Y + XY\overline{Z}$

2.
$$(\overline{A} + \overline{C})(\overline{A} + C)(A + B + \overline{C}D)$$

3.
$$(X + Y)(\overline{X} + Y)$$

4. $[A\overline{B}(C + BD) + \overline{A}\overline{B}]C$

to one literal to four literals. to two literals to two literals

Q3) Draw the logic diagram of the following Boolean function without simplifying them

- 1. $F1 = B\overline{C} + AD$
- 2. $F2 = B(\bar{C} + A)$
- 3. F3 = $\overline{(X + Y)}(\overline{X} + Y)$

14.Canonical and Standard forms:

12. A Canonical form: canonical forms (Sum of Minterms or Product of Maxterms) are used to obtain the function from the given truth table

х	у	Z	Minterms	Notation	Maxterms	Notation
0	0	0	x'y'z'	m_0	(x+y+z)	M_0
0	0	1	x'y'z	m_1	(x+y+z')	M_1
0	1	0	x'yz'	m ₂	(x+y'+z)	M ₂
0	1	1	x'yz	m ₃	(x+y'+z')	M ₃
1	0	0	xy'z'	m_4	(x'+y+z)	M_4
1	0	1	xy'z	m5	(x'+y+z')	M5
1	1	0	xyz'	m_6	(x'+y'+z)	M6
1	1	1	xyz	m7	(x'+y'+z')	M ₇
			Variable		Variable	
			Primed if =0		Primed if =1	
			Imprimed=1		Imprimed=0	

12. A .1 Sum of Minterms:

A Boolean function may be expressed algebraically as a sum of minterms from a given truth table by:

Step1: forming a minterm for each combination of the variables which produce 1 in the function.

Step2: OR all of the minterms in step1.

Example: From the given truth table express F as a sum of minterms

Given				Solution		
Inputs		ts	Output	Step1	Step2	
Х	у	Z	F	minterms	Sum of minterms	
0	0	0	0		F = x'y'z + x'yz + xyz	
0	0	1	1	x'y'z	$F=m_1+m_3+m_7$	
0	1	0	0		$F(x,y,z) = \Sigma(1,3,7)$	
0	1	1	1	x'yz		
1	0	0	0			
1	0	1	0			
1	1	0	0			
1	1	1	1	XYZ		

From the table F' can be expressed as a sum of minterms as follows:

Step1: forming a minterm for each combination of the variables which produce 0 in the function.

Step2: OR all of the minterms in step1.

Example: From the given truth table express F' as a sum of minterms

Given				Solution			
Inputs Input		Inputs	Step1 Step2				
Х	у	z	F	minterms	Sum of minterms		
0	0	0	0	x'y'z'	F'=x'y'z'+x'yz'+xy'z'+xy'z+xyz'		
0	0	1	1		$F'=m_0+m_2+m_4+m_5+m_6$		
0	1	0	0	x'yz'	$F'(x,y,z) = \Sigma(0,2,4,5,6)$		
0	1	1	1				
1	0	0	0	xy'z'			
1	0	1	0	xy'z			
1	1	0	0	xyz'			
1	1	1	1				

12. A .2 Product of Maxterms:

A Boolean function may be expressed algebraically as a product of maxterms from a given truth table by:

Step1: forming a maxterms for each combination of the variables which produce 0 in the function.

Step2: form the AND of all the maxterms in step1.

Example: From the given truth table express F as a product of maxterms

Given			en	Solution			
Inputs In		Inputs	Step1	Step2			
Х	у	Z	F	maxterms	Product of maxterms		
0	0	0	0	(x+y+z)	F = (x+y+z) (x+y'+z) (x'+y+z) (x'+y+z') (x'+y'+z)		
0	0	1	1		$F = M_0.M_2.M_4.M_5.M_6$		
0	1	0	0	(x+y'+z)	$F(x,y,z)=\Pi(0,2,4,5,6)$		
0	1	1	1				
1	0	0	0	(x'+y+z)			
1	0	1	0	(x'+y+z')			
1	1	0	0	(x'+y'+z)			
1	1	1	1				

From the table F' can be expressed as follows:

Step1: forming a maxterm for each combination of the variables which produce 1 in the function.

Step2: form the AND of all the maxterms in step1.

	(Giv	en	Solution			
Inputs		Inputs	Step1	Step2			
Х	у	Z	F	maxterms	Product of maxterms		
0	0	0	0		F'=(x+y+z')(x+y'+z')(x'+y'+z')		
0	0	1	1	(x+y+z')	$F'=M_{1.}M_{3.}M_{7}$		
0	1	0	0		$F'(x,y,z) = \Pi(1,3,7)$		
0	1	1	1	(x+y'+z')			
1	0	0	0				
1	0	1	0				
1	1	0	0				
1	1	1	1	(x'+y'+z')			

Example: From the given truth table express F' as a product of maxterms

12. B. Standard Forms:

Sum terms: single variable or logical sum of several variables such as (A, B, (x+y), (A+C')). Product terms: single variable or logical product of several variables such as (x, y, AB', CD')

Note: the expression x+y'z (not sum term nor product terms)

12. B.1. Sum of Products (SOP): is a Boolean expression containing AND terms, called product terms, of one or more literals each. The sum denotes the ORing of these terms. An example of a function expressed as a sum of product is F1=y'+xy+x'yz'

The expression contains three product terms (y' one literal, xy two literals and x'yz' three literals). Their sum is in effect an OR operation. The logic diagram if a sum-of-product expression consist of a group of AND gates followed by a single OR gate.

12. B.2 Product of Sums (POS): is a Boolean expression containing OR terms, called sum terms, of one or more literals each. The product denotes the ANDing of these terms. An example of a function expressed as a product of sum is F2=x(y'+z)(x'+y+z)

The expression contains three sum terms (x one literal, y'+z two literals and x'+y+z three literals). The product is an AND operation. The logic diagram if a product-of-sum expression consist of a group of OR gates followed by a single AND gate.



Two-level implementation

Note: a Boolean function may be expressed in a nonstandard form

Ex: F = (AB + CD) (A'B' + C'D') is neither in sum of products nor product of sums. It can be change to the standard form using the distributive law:

F = ABA'B' + ABC'D' + CDA'B' + CDC'D'

= 0 + ABC'D' + A'B'CD + 0

F = ABC'D' + A'B'CD sum of products

H.W. Express F in a product of sums.

Example: From the given truth table express F as a sum of minterms then simplify as a sum of product

Given						
Х	у	Z	F			
0	0	0	0			
0	0	1	0			
0	1	0	1			
0	1	1	1			
1	0	0	0			
1	0	1	0			
1	1	0	1			
1	1	1	0			

Solution: the function equal to 1 in $\{(2,x'yz'),(3,x'yz),(6,xyz')\}$

So F=x'yz'+x'yz+xyz' (Sum of Minterms)

Simplification of F

 $F = \underline{x'yz'} + \underline{x'yz} + xyz'$

- =x'y(z'+z)+xyz' (distributive law)
- =x'y.1+xyz' (complement definition)

=x'y+xyz' (identity element)

=y(x'+xz') (distributive law)

=y(x'+x)(x'+z') (distributive law)

- =y.1.(x'+z') (complement definition)
- =y(x'+z') (identity element)
- =x'y+yz' (distributive law)



Logic Circuit of F = x'y + yz'

Example: From the given truth table express F

as a product of maxterms then simplify as a product of sum

Solution: the function equal to 0 in $\{(0,x+y+z),(1,x+y+z'),(4,x'+y+z),(5,x'+y+z'),(7,x'+y'+z')\}$

So F=(x+y+z)(x+y+z')(x'+y+z)(x'+y+z') product of maxterms

Simplification of F

F = (x+y+z) (x+y+z') (x'+y+z) (x'+y+z') (x'+y'+z')

=[(x+y)+zz'] [(x'+y)+zz	z')] (x'+y'+z')	(distributive law)	
=[(x+y)+0] [(x'+y)+0] ((x'+y'+z')	(complement definition)	
$= (\underline{x+y}) (\underline{x'+y}) (x'+y'+z')$		(identity element)	
=(y+xx') (x'+y'+z')		(distributive law)	
= (y+0) (x'+y'+z')		(complement definition)	
= y(x'+y'+z')		(identity element)	
= x'y+yy'+yz'		(distributive law)	
=x'y+0+yz'		(complement definition)	
=x'y+yz'	(ide	entity element)	
=y(x'+z')	(distributive law)	to convert the function from SOP	to POS



Logic Circuit of F=y(x'+z')

12.C convert functions to the canonical forms:

12.C.1 conversion to sum of minterms:

It is sometimes convenient to express function in its sum of minterms form by:

- a. Expanding the expression in to sum of AND terms (SOP)
- b. Each AND term is inspected to see if it contains all the variables. If it missing one or more variables, it is ANDed with an expression (x+x'), where x is one of the missing variable

Example: Express the Boolean function F=A+B'C in a sum of minterms.

<u>Solution</u>: the function F has three variables A,B and C. it is in SOP standard form the first product term (A) missing two variable (B,C); therefore

A = A (B+B') = AB + AB'

This terms still missing one variable (C):

A = AB(C+C') + AB'(C+C')

= ABC + ABC' + AB'C + AB'C'

The second term (B'C) missing one variable (A):

B'C = B'C (A+A') = B'CA + B'CA' rearrange the variable alphabetically

B'C = AB'C + A'B'C

Combining all terms, we have:

F = A + B'C

 $= ABC + ABC' + \underline{AB'C} + AB'C' + \underline{AB'C} + A'B'C$

Since (x+x=x) we can eliminate one of the underlined term

F = A'B'C + AB'C' + AB'C + ABC' + ABC

 $=\!m_1+m_4+\ m_5+m_6+m_7$

 $F(A,B,C)=\Sigma(1,4,5,6,7)$

12.C.2 Conversion to product of maxterms:

To express function in its product of maxterms form by:

- a. Expanding the expression in to product of **OR** terms (POS), using distributive law
- b. Each OR term is inspected to see if it contains all the variables. If it missing one or more variables, it is **OR**ed with an expression (xx'), where x is one of the missing variable

Example: Express the Boolean function F = xy + x'z in a product of maxtermes.

First: convert the function into OR terms (POS) by using distributive law:

$$F = xy + x'z = let a = xy$$

$$F = a + x'z = (a + x') (a + z) = (xy + x') (xy + z)$$

$$= (x' + x) (x' + y) (z + x) (z + y)$$

$$F = (x' + y) (z + x) (z + y) POS$$

The function has three variables x, y and z. each OR term is missing one variable; therefore:

$$(x' + y) = (x' + y) + zz' = (x' + y + z) (x' + y + z')$$
$$(z + x) = (z + x) + yy' = (z + x + y) (z + x + y') = (x + y + z) (x + y' + z)$$
$$(z + y) = (z + y) + xx' = (z + y + x) (z + y + x') = (x + y + z) (x' + y + z)$$

Combining all terms and removing all those that appear more than once, we finally obtain:

$$\begin{split} F &= (\ x + y + z \) \ (\ x + y' + z \) \ (\ x' + y + z \) \ (\ x' + y + z' \) \\ &= M_0 \ M_2 \ \ M_4 \ M_5 \end{split}$$

 $F(x,y,z) = \Pi (0, 2, 4, 5)$

12.C.3 Conversions between Canonical forms:

To convert from one canonical form to another: interchanging the symbols Π and Σ then list those numbers missing in the original form. In order to find the missing terms, one must realize the total number of minterms and maxterms is 2^n , where n is the number of binary variables in the function.

Example: convert the Boolean function $F(x,y,z) = \Sigma(0,2,4,5)$ to the other canonical form.

The number of variables is three (x, y, z), therefore the total numbers is in the range $(0..2^3-1)=(0..7)$ therefore, $F(x,y,z)=\Pi(1,3,6,7)$

Lecture 4

15.Other Logical Operations:

Name	Graphical symbol	Algebraic function	Truth table
AND	x y	F=x.y	x y F 0 0 0 0 1 0 1 0 0 1 1 1
OR	x y	F=x+y	$\begin{array}{c ccc} x & y & F \\ \hline 0 & 0 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 1 \end{array}$
NOT, Inverter	x		$\begin{array}{c c} x & x' \\ \hline 0 & 1 \\ 1 & 0 \end{array}$

Buffer	x X		x x 0 0 1 1
NAND	x y	F= (xy)' = x↑y	x y F 0 0 1 0 1 1 1 0 1 1 1 0
NOR	x y	$F=(x+y)'$ $= x \downarrow y$	x y F 0 0 1 0 1 0 1 0 0 1 1 0
XOR	x y	F=x'y+xy' =x⊕y	x y F 0 0 0 0 1 1 1 0 1 1 1 0
XNOR	x y	$F=x'y'+xy$ $=(x \bigoplus y)'$ $= x \odot y$	x y F 0 0 1 0 1 0 1 0 0 1 1 1

Exclusive OR (XOR): odd function equal to 1 if the numbers the input variables have an odd number of 1's and 0 otherwise. The construction of 2-input Exclusive-OR function is shown below. It is normally implemented by cascading 2-input gates, as shown in below:



The following identities apply to Exclusive –OR operation:

 $x \oplus 0=x$, $x \oplus x=0$, $x \oplus y' = x' \oplus y = (x \oplus y)'$

 $x \oplus 1{=}x' \qquad , x \oplus x'{=}1 \quad ,$

Equivalence or Exclusive NOR: even function equal to 1 if the number of 0's in the input variables are even and 0 otherwise.

XOR and Equivalence are both commutative and associative.

 $x\uparrow y=(xy)'=x'+y'$ $y\uparrow x=(yx)'=y'+x'=x'+y'$ \therefore NAND is commutative $x\downarrow y=(x+y)'=x'y'$ $y\downarrow x=(y+x)'=y'x'=x'y'$ \therefore NOR is commutative $(x\uparrow y)\uparrow z=(xy)'\uparrow z=((xy)'z)'=(xy)''+z'=xy+z'$ $x\uparrow (y\uparrow z)=x\uparrow (yz)'=(x'(yz)')'=x'+(yz)''=x'+yz$ \therefore NAND is not associative.

H.W. Neither prove that NOR is associative or not.

16.NAND and NOR gates.

Two other gates, NAND and NOR are often used in computer. To show any function can be implemented with NAND or NOR gates, we need only show that the logical operations of AND & OR can be obtained from NAND or NOR only.

	AND gate	OR gate
Using NAND	$x = \sum_{y = 1}^{\infty} (x \cdot y)' = x \cdot y$	$\begin{array}{c} x \\ y \\ y \\ \end{array} \begin{array}{c} x' \\ y' \\ y' \\ \end{array} \begin{array}{c} (x'.y')' = x+y \\ y' \\ \end{array}$
Using NOR	$x \xrightarrow{x'} y' \xrightarrow{(x'+y')'=x''.y''=x.y}$	x y $(x+y)' = (x+y)$

13. Map Simplification:

Boolean function may be simplified by algebraic means, but this procedure lacks specific rules to predict each succeeding step in the manipulation process. The map method provides a simple straight forward procedure for minimizing Boolean functions. The map is a diagram made up of squares each square represents one minterms.

13.1 Two and Three variables maps:

in two variable map, there are 4 minterms hence the map consists of four squares , one for each minterm.

Example: simplify F using map method, where $F(x,y)=\sum(1,2,3)$



Example: simplify F using map method, where $F(x,y)=\sum(3)$



A three variable map is shown below, note that the minterms are arranged, not in binary sequence, the characteristic of this sequence is that the only one bit changed from (1 to 0) or from (0 to 1) in the listing sequence.

<u> </u>	v7.		У						
x	<u>, ~ 00</u>	01	′ 11	10 '	.				
0	x'y'z'	x'y'z	x'yz	x'yz'		m ₀	m ₁	m <u>3</u>	m ₂
x [1	xy'z'	xy'z	xyz	xyz'		m4	m5	m ₇	m ₆
		2	Z						

The basic property proposed by the adjacent squares that only two adjacent squares in the map differ by only one variable which is primed in one square and unprimed in the other. For example m6 and m7 hence, the sum of two minterms in the adjacent square can be simplified to a simple AND term consisting of only two literals

m6+m7= xyz' + xyz = xy (z'+z) = xy . 1 = xy Example: simplify F using map method, where $F(x,y,z)=\sum(0,1,4,6,7)$



Example: simplify F using map method, where $F(x,y,z)=\sum(3,4,6,7)$



Example: simplify F using map method, where $F(x,y,z)=\sum(0,2,4,6)$



Example: simplify F using map method, where $F(x,y,z)=\sum(1,3,5,6,7)$



Note:- any combination of 4 adjacent squares in the 3-variables map, which represents the ORing of four adjacent minterms will result in an expression of only one literals.

Example: simplify F using map method,

where F = A'B'C' + A'C + A'B + AB'C + BC

Sol.: the terms need to be expressed as a sum of minterms as explain before, so A'C missing B, A'B missing C and BC missing A

F = A'B'C' + A'C (B+B') + A'B(C+C') + AB'C + BC(A+A')

= A'B'C' + A'BC + A'B'C + A'BC + A'BC' + AB'C + ABC + A'BC

= A'B'C' + A'B'C + A'BC' + A'BC + AB'C + ABC

: $F(A,B,C)=\sum(0,1,2,3,5,7)$ and the simplification of F using the map methods is as follows:



13.2 Four variables map:-

The combinations of adjacent squares that is useful during the simplification process easily determined for inspection of the 4-variable map

- (2^0) One square represents one minterm, given a term of 4 literals
- \checkmark (2¹)Two adjacent squares represents a term of 3 literals.
- \checkmark (2²)Four adjacent squares represents a term of 2 literals.
- \blacksquare (2³)Eight adjacent squares represents a term of 1 literal.
- \checkmark (2⁴)Sixteen adjacent squares the function equal to 1 (constant)



Example: simplify F using map method, where $F(A,B,C,D) = \sum (0,1,2,4,5,6,8,9,12,13,14)$



Example: simplify F using map method, where $F(A,B,C,D)=\sum(0,1,2,6,8,9,10)$



Example: simplify F using map method,

Where, $F(w,x,y,z) = \sum (2,3,7,8,9,10,11,15)$



14. Product of Sum Simplification.

The minimized Boolean function derived from the map in all previous example were expressed in the sum of product form, with a minor or modification the product of sums forms can be obtained.

Example: simplify F using map method as a) sum of products b) product of sums, where $F(A,B,C,D)=\sum (2,3,4,5,10,11,12,13,14,15)$



15. Don't care Conditions:

The don't care conditions can be used on a map to provide further simplification of the function. To distinguish the don't care conditions from 1's and 0's, an X will be used. When choosing the adjacent square to simplify the function in a map, the X's may be assumed to be either (0 or 1) whichever gives the simple expression.

Example: simplify F using map method as a) sum of products b) product of sums, where $F(A,B,C,D)=\sum(4,10,11,12,14,15)$ and the don't care conditions $d(A,B,C,D)=\sum(2,3,5,13)$



16. NAND and NOR implementations.

16.1. NAND circuits:

The Boolean functions can be implemented with two levels of NAND gates by:

- a) Simplifying the function and express in sum of product term.
- b) Draw NAND gate for each product term of expression that has at least two literals. The inputs of each of each NAND gates are the literals of the term. This constitutes a group of first-level gates.
- c) Draw single gate using the AND-invert graphic symbol in the second level, with inputs coming from outputs of the first level gates.
- d) A term with single literal requires an inverter in the first level.

Example: implement F with NAND gates, where $F(x,y,z)=\sum(1,2,3,4,5,7)$



16.2. NOR circuits:

The Boolean functions can be implemented with two levels of NOR gates by:

- a) Simplifying the function and express in product of sums term.
- b) Draw NOR gate for each sum term of expression that has at least two literals. The inputs of each of each NOR gates are the literals of the term. This constitutes a group of first-level gates.
- c) Draw single gate using the OR-invert graphic symbol in the second level, with inputs coming from outputs of the first level gates.
- d) A term with single literal requires an inverter in the first level.

Example: implement F with NOR gates, where $F(x,y,z)=\sum(1,3,4,5)$



Lecture 5

17.Combinational Circuits

Logic circuits whose outputs at any time are determined directly and only from the present input combination



A. Analysis Procedure:

Boolean Expression Approach:

- Label all gate outputs that are functions of the input variables only. Determine the functions.
- Label all gate outputs that are functions of the input variables and previously labeled gate outputs, and find the functions.
- E Repeat previous step until all the primary outputs are obtained.

<u>Ex.1</u> Analyze the circuit shown in the following figure:



Solution: Step1:



HW. Derive the T.T. of the F1 and F2

B. Design Procedure:

The steps to design combinational circuits are as the following:

- 1. Understand the problem
- 2. Determine the number of input and output variables that are needed.
- 3. Give symbols for the stated input and output.
- 4. Construct a truth table that defines the relationship between the input and output.
- 5. Obtain the Boolean function or the logical expression from the truth table in step 4, using K-map map or other known methods.
- 6. Draw a logic circuit based on the expression obtained from step 5 above.

Ex.2. Design a circuit that accept 3-bit binary number and produce 1 if the number of 0's greater than the number of 1's in the input combination and produce 0 otherwise. **Solution:**

Generate the truth table

Inputs N0. of 0's and 1's in the input combinations		and 1's in the mbinations	Condition	Output		
2 ²	21	20	N0. of 0's	N0. of 1's	Is N0. Of 0's > N0. of 1's?	F
0	0	0	3	0	Is (3>0)=T	1
0	0	1	2	1	Is (2>1)=T	1
0	1	0	2	1	Is (2>1)=T	1
0	1	1	1	2	Is (1>2)=F	0
1	0	0	2	1	Is (2>1)=T	1
1	0	1	1	2	Is (1>2)=F	0
1	1	0	1	2	Is (1>2)=F	0
1	1	1	0	3	Is (0>3)=F	0

Iı	nput	Output	
Х	Y	Ζ	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

- Express each output function as sum of minterms: $F(X,Y,Z)=\sum(0,1,2,4)$
- Simplify each output function using (Boolean algebra or Map method)



Draw the logic circuit of
 the output function

Ex.3. Design a combinational circuit that accepts 3-bit binary number and produces the number of 1's in each input combination in binary.

0 1	
SO	intion•
001	unon.

Inputs			Output	
2^{2}	2 ¹	2^{0}	N0. Of 1's	
0	0	0	0	
0	0	1	1	
0	1	0	1	
0	1	1	2	
1	0	0	1	
1	0	1	2	
1	1	0	2	
1	1	1	3	

Number of output variables=2 {since maximum value =3 needs 2 binary digits to be written $(3)_{10}=(11)_2$

Assign symbols to the input and output columns

Inputs			Outputs in binary				Ι
2^{2}	2^{1}	20	2^{1}	20		Х	
0	0	0	0	0		0	
0	0	1	0	1		0	
0	1	0	0	1		0	
0	1	1	1	0		0	
1	0	0	0	1		1	
1	0	1	1	0		1	
1	1	0	1	0		1	
1	1	1	1	1		1	

	Inputs	Outputs in binary		
Х	у	Z	А	В
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Express each output function as sum of minterms: $A(X,Y,Z)=\sum(3,5,6,7)$

 $B(X,Y,Z)=\sum(1,2,4,7)$

Simplify each output function (A and B) using Map method

: There are 3 input variables \therefore use 3-Var. map $2^3=8$ squares

Draw 2-maps (one for each output functions)



$$A = xz + yz + xy$$

$$B = \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xyz$$

$$B = \bar{x}(y\bar{z} + \bar{y}z) + x(\bar{y}\bar{z} + xy)$$

$$B = \bar{x}(y \oplus z) + x(y \odot z)$$

Let $A = (y \oplus z) \quad \therefore \bar{A} = (y \odot z)$
 $B = \bar{x}A + x\bar{A}$
 $B = x \oplus A$

$B = x \oplus y \oplus z$

Draw the circuit



Lecture 6

18. Adder

18.1. Half Adder (HA)

A half adder is a logical circuit that performs an addition operation on two binary bits.

Х	0	0	1	1		ſ
	+	+	+	+		
Y	0	1	0	1		
	Ш	=	Ш	Ш		I
Carry				1		
Sum	0	1	1	0		
						L

inp	uts		Outputs in		
			Binary		
21	2^{0}		21	20	
Х	Y	addition	Carry	Sum	Minterms
0	0	0	0	0	
0	1	1	0	1	$\overline{\mathbf{X}}\mathbf{Y}\left(\mathbf{S}\right)$
1	0	1	0	1	$X\overline{Y}(S)$
1	1	2	1	0	XY (C)



18.2. Full adder (FA)

A full adder is a logical circuit that performs the arithmetic sum of three binary bits (two significant and the previous carry)





Design FA using 2-HA and external OR gate

2.3Binary Adder:

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adder in cascaded.



19. Magnitude Comparator

The comparison of two numbers is an operation that determine if one number is greater than, less than, or equal to the other number. A magnitude comparator is combinational circuit that compares two numbers, A and B, and determines their relative magnitude. The outcome of the comparison is specified by three binary variables that indicate whether A>B, A=B, and A<B.

The circuit of comparing two n-bit binary numbers has 2^{2n} entries in the truth table

19.1. 1-bit comparator circuit

Α	B	A>B	A <b< th=""><th>A=B</th></b<>	A=B
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1



19.2. **2-bit comparator circuit**

A comparator circuit processes a certain amount of regularity. Digital function which processes an inherent well-defined regularity can usually be designed by means of an algorithmic procedure if one is found to exist. An algorithm is a procedure that specifies a finite set of steps which, if followed, give the solution to the problem. We illustrate this method by deriving an algorithm for the design of a 2-bit magnitude comparator.

Consider two numbers A and B where

$$\begin{array}{ll} A= \ A_1 \ A_0 \\ B= \ B_1 \ B_0 \end{array}$$

• The two numbers are equal if all pairs of significant digit are equal (i.e. $A_1 = B_1$ and $A_0 = B_0$)

$$X_1 = (A_1 = B_1)$$

 $X_0 = (A_0 = B_0)$

- A greater than B if $(A_1 > B_1)$ OR $(A_1 = B_1)$ AND $(A_0 > B_0)$
- A less than B if $(A_1 < B_1)$ OR $(A_1 = B_1)$ AND $(A_0 < B_0)$

 $(A=B) = X_1 X_0$ (A>B)= (A_1>B_1) + X_1 (A_0>B_0) (A<B)= (A_1<B_1) + X_1 (A_0<B_0)

The circuit of <u>**2-bit comparator**</u> is derived by repeating 1-bit comparator circuit for each pair of numbers (i.e. (A_1, B_1) and (A_0, B_0)) as shown in the following figure



19.3. **4-bit comparator circuit**

Consider two numbers A and B where

 $A = A_3 A_2 A_1 A_0$ $B = B_3 B_2 B_1 B_0$

• The two numbers are equal if all pairs of significant digit are equal (i.e. $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$ and $A_0 = B_0$)

 $X_i = (Ai = Bi)$ where i=0,1,2,3

- A greater than B if $(A_3 > B_3)$ <u>OR</u> X_3 AND $(A_2 > B_2)$ <u>OR</u> $X_3 X_2$ AND $(A_1 > B_1)$ <u>OR</u> $X_3 X_2 X_1$ AND $(A_0 > B_0)$
- A less than B if (A₃<B₃) <u>OR</u> X₃ AND (A₂<B₂) <u>OR</u> X₃ X₂ AND (A₁<B₁) <u>OR</u> X₃ X₂ X₁ AND (A₀<B₀) (A=B)= X₃ X₂ X₁ X₀ (A>B)= (A₃>B₃) + X₃(A₂>B₂) +X₃ X₂ (A₁>B₁) +X₃ X₂ X₁ (A₀>B₀) (A<B)= (A₃<B₃) + X₃(A₂<B₂) +X₃ X₂ (A₁<B₁) +X₃ X₂ X₁ (A₀<B₀)

The circuit of <u>4-bit comparator</u> is derived by repeating 1-bit comparator circuit for each pair of numbers (i.e. $(A_3, B_3), (A_2, B_2), (A_1, B_1)$ and (A_0, B_0)) as shown in the following figure



Lecture 7

20. Decoder

A binary code of n bits is capable of representing up to 2^n distinct binary code. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the *n-bit* decoded information has unused or don't-care combinations, the decoder output will have less than 2^n outputs. <u>Ex6.</u> Design 2-to-4 line decoder



<u>Ex7.</u> Design 3-to-8 line decoder or design binary to Octal decoder

- How many bits in binary needs to configure one Octal digit? Three binary bits needs to configure one octal digit, thus the input variables are three
- The octal system coefficients are (0,1,2,3,4,5,6,7), thus the output lines are eights

			Iı	npu	ts				Out	puts			
			X	у	Z	D7	D6	D5	D4	D3	D2	D1	D0
Х —	3-to-8		0	0	0	0	0	0	0	0	0	0	1
Y —	line	D 4	0	0	1	0	0	0	0	0	0	1	0
Ž —	ime	D3	0	1	0	0	0	0	0	0	1	0	0
	Decoder	$-D^2$	0	1	1	0	0	0	0	1	0	0	0
			1	0	0	0	0	0	1	0	0	0	0
I			1	0	1	0	0	1	0	0	0	0	0
			1	1	0	0	1	0	0	0	0	0	0
			1	1	1	1	0	0	0	0	0	0	0



Ex8. Design BCD-to-Decimal decoder

The elements of information in this case are ten decimal digits represented by BCD code. The code itself has four bits. Therefore, the decoder should have four inputs to accept the coded digit and ten outputs, one for each decimal digit. This will give a 4-line to 10-line BCD-to-Decimal decoder





21.Multiplexer:

Is also called the data selector, since it selects one of many inputs. A digital multiplexer (MUX) is a combinational circuit that selects binary information from one of many inputs lines and directs it to a single output line. The selection of particular input lines is controlled by a set of selection lines. Normally there are 2^n input lines and *n* selection lines whose bit combinations determine which input is selected.

Ex12. Design 2-to-1 MUX 2 is the number of the input variable (I₁,I₀) $2=2^n \rightarrow n=1$ where n is the selection variable (S)



Ex13. Design 4-to-1 MUX

4 is the number of the input variable (I_3, I_2, I_1, I_0) 4=2ⁿ =2² \rightarrow n=2 where n is the selection variable (S_1, S_0)



The AND gates and inverter in multiplexer resemble a decoder circuit and they decode the input selection lines. In general 2^n to 1 line MUX is constructed from *n*-to- 2^n decoder by adding to its 2^n input lines, one to each input lines.(see Ex12. 2-inputs s_{1s0}, 4 AND gets each has 3- input variables (s₁, s₀ and either { I₃,I₂,I₁,I₀}).

The size of a multiplexer is specified by the 2^n of its input lines and a single output lines. It is then implied that it also contain n selection lines.

21.1. Boolean Function Implementation

A decoder can be used to implement a Boolean function by employing an external OR gate. The multiplexer is a decoder with OR gate already available.

If we have a Boolean function of n+1 variable, we take n of these variables and connect them to the selection lines of a multiplexer. The remaining single variable of the function is used for the input lines of the multiplexer.

<u>Ex.</u> Implement $F(A,B,C)=\sum(1,3,5,6)$ using MUX, select A as input variable.

 \therefore A is used as input variable. \therefore The reaming two variables (B,C) are used as selection lines

 \therefore n=2 is the number of selection lines (B,C) $\rightarrow 2^2=4$ is the number of input lines (I₃,I₂,I₁,I₀) that must be written in terms of input variable (A)

Μ	interms		A	B	С	F				In	pu	t lin	es	
	0		0	0	0	0				Io	\mathbf{I}_1	I_2	I ₃	
	1	Ā	0	0	1	1	It	•	Ā	0	(1)	2	3	
	2	А	0	1	0	0	npu	var	Λ	4	<u>ि</u>	6	7	
	3		0	1	1	1			A	4	9	0	/	
	4		1	0	0	0				0	1	Α	Ā	
	5	Λ	1	0	1	1								
	6	A	1	1	0	1								
	7		1	1	1	0								
	Selection	n-liı	ne	Out	put						Iı	nput	t line	5
	В	С		F	7					.	1	Ŧ	<u>-</u>	.
	0	0		I ₀ =	=0					I()	\mathbf{I}_1	12	13
	0	1		I_1	=1	_			Ā			\bigcirc	0	\bigcirc
	1	0		I ₂ =	=A	_	put	ar.			<u> </u>	U	0	
	1	1		I ₃ =	=A		In	Ņ	Α	0)	(1)	()	0
										0)	1	Α	Ā



<u>Ex.</u> Implement $F(A,B,C,D)=\sum(0,1,3,4,8,9,15)$ using MUX, select B as input variable. \therefore B is used as input variable. \therefore The reaming three variables (A,C,D) are used as selection lines

∴ n=3 is the number of selection lines (A,C,D) $\rightarrow 2^3=8$ is the number of input lines (I₇,I₆,I₅,1₄,I₃,I₂,I₁,I₀) that must be written in terms of input variable (B)

Ι	Mint	erms		Α	В	С	D	F				Iı	nput	line	es				
	()		0	0	0	0					Io	I.	Ŀ	I2	L	L	L	I ₇
	1	1	Ē	0	0	0	1				11			12	$\overline{1}_{3}$			16	1/
	2	2	В	0	0	1	0			put	B	\bigcirc	U	2	3	8	9	10	11
		3		0	0	1	1			[n]	B	4	5	6	7	12	13	14	(5)
	4	1		0	1	0	0						=	0	=	=	=	0	
	4	5	п	0	1	0	1					1	В	0	B	В	В	0	B
	6	5	В	0	1	1	0												
	7	7		0	1	1	1												
	8	3		1	0	0	0												
	ç)	₽	1	0	0	1												
	1	0	D	1	0	1	0												
	1	1		1	0	1	1												
	1	2		1	1	0	0												
	1	3	п	1	1	0	1												
	1	4	D	1	1	1	0												
	1	5		1	1	1	1												
S	Selec	tion-l	ine	Out	put]	Inpu	ıt lir	nes				
	A	С	D	F	7							L	T.	L	L	L	I.	L	I-
	0	0	0	I ₀ =	=1						5						15	16	1/
	0	0	1	I ₁ =	=B					put	<u>н</u>	U		0			U	0	0
	0	1	0	I2=	=0					In	[₽] B		0	0	0	0	0	0	(1)
	0	1	1	I3=	= <u>B</u>	-							=		=	=	5	0	
	1	0	0	I ₄ =	= <u>B</u>	-							B	0	B	B	B	0	В
	1	0	1	l5=	=B	-													
_	1	1	0	16= T	=0 D	-													
	1	1	1	17=	=В				1										



<u>Ex.</u> Implement F-A using Dual-MUX, let the most significant variable is the input variable.

I	Inputs Outputs in bina		n binary	• The output functions must be written as					
Х	у	Z	С	S	S.O. minterms as:				
0	0	0	0	0	$C(x,y,z) = \sum (3,5,6,7)$				
0	0	1	0	1	$S(x,y,z) = \sum (1,2,4,7)$				
0	1	0	0	1					
0	1	1	1	0					
1	0	0	0	1					
1	0	1	1	0					
1	1	0	1	0					
1	1	1	1	1					

 \because x is used as input variable. \div the reaming two variables (y,z) are used as selection lines \rightarrow n=2

 $2^2=4$ is the number of input lines(I_3,I_2,I_1,I_0) that must be written in terms of input variable (x)

<u>C</u>		I	nput	line	es	<u>S</u>	I	Input lines						
		I ₀	I_1	I_2	I ₃		I ₀	I_1	I_2	I ₃				
ut r.	\bar{x}	0	1	2	3	ti : <i>x</i>	0	1	2	3				
Inp	x	4	5	6	7	Inp x	4	5	6	0				
		0	x	x	1		x	\overline{x}	\bar{x}	x				

[
Selection	on-lines	Out	tput	010
у	Z	С	S	$\mathbf{x} - I_1 - I_1$
0	0	$I_0=0$	$I_0 = x$	$I_2 \qquad I_2 \qquad I_3 \qquad I_4 \qquad I_7 $
0	1	$I_1 = x$	$I_1 = \bar{x}$	
1	0	$I_2 = x$	$I_2 = \bar{x}$	113
1	1	I ₃ =1	$I_3 = x$	
				$\begin{array}{c} y \\ z \\ \hline \\ \hline$

Lecture 8

22.Sequential Circuits



Block diagram of sequential circuit

As shown in the block diagram of a sequential circuit. It consists of a combinational circuit to which storage elements are connected to form a feedback path. The storage elements are devices capable of storing binary information. The binary information stored in these elements at any given time defines the *state* of the sequential circuit at that time. The sequential circuit receives binary information from external inputs that, together with the present state of the storage elements, determine the binary value of the outputs. These external inputs also determine the condition for changing the state in the storage elements.

- The block diagram demonstrates that the outputs in a sequential circuit are a function not only of the inputs, but also of the present state of the storage elements.
- The next state of the storage elements is also a function of external inputs and the present state. Thus, a sequential circuit is specified by a time sequence of inputs, outputs, and internal states.
- In contrast, the outputs of combinational logic depend only on the present values of the inputs.

There are two main types of sequential circuits, and their classification is a function of the timing of their signals. A synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time. The behavior of an asynchronous sequential circuit depends upon the input signals at any instant of time and the order in which the inputs change.

A synchronous sequential circuit employs signals that affect the storage elements at only discrete instants of time. Synchronization is achieved by a timing device called a clock *generator*, which provides a clock signal having the form of a periodic train of *clock pulses*. Synchronous sequential circuits that use clock pulses to control storage elements are called clocked *sequential circuits* The storage elements (memory) used in clocked sequential circuits are called flip *flops*. A flip-flop is a binary storage device capable of storing one bit of information. In a stable state, the output of a flip-flop is either 0 or 1. A sequential circuit may use many flip-flops to store as many bits as necessary

22.1 Basic Flip-Flops

The basic flip-flop can be constructed from two cross-coupled NOR gates or two cross-coupled NAND gates, and two inputs labeled S for set and R for reset.



20.2 Clocked SR Flip-Flop



20.3 D Flip-Flop

One way to eliminate the undesirable condition of the indeterminate state in the SR flip-flop is to ensure that inputs S and R are never equal to 1 at the same time. This is done in the D flip-flop.



20.4 JK Flip-Flop



Funct	tion T	able w	when Cl	P=1			I	
Q	J	Κ	Qt+	1				
0	0	0	0					1
0	0	1	0					T
0	1	0	1			ϱ		OK'
0	1	1	1				<i>K</i>	
1	0	0	1				Ot+1 = O'J + O'	DK'
1	0	1	0				Chana stanistic I	
1	1	0	1				Characteristic f	Lquation
1	1	1	0					
					F	unct	ion Table	
				CP	T	Κ	Ot+1	
					J		211	
				0	X	X	Q No change	
				0 1	у Х 0	X 0	Q No change Q No change	
				0 1 1	y X 0 0	X 0 1	Q No change Q No change 0	
				$\begin{array}{c} 0 \\ 1 \\ 1 \\ 1 \\ \end{array}$	J X 0 0 1	X 0 1 0	Q No change Q No change 0 1	

20.5 T Flip-Flop

