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A PROPOSED DUAL SIZE DESIGN FOR ENERGY MINIMIZATION IN SUB-THRESHOLD CIRCUITS

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Abstract

Sub-threshold operation has received a lot of attention in limited performance applications.However, energy optimization of sub-threshold circuits should be performed with the concern of the performance limitation of such circuit. In this paper, a dual size design is proposed for energy minimization of sub-threshold CMOS circuits. The optimal downsizing factor is determined and assigned for some gates on the off-critical paths to minimize the energy at the maximum allowable performance. This assignment is performed using the proposed slack based genetic algorithm which is a heuristic-mixed evolutionary algorithm. Some gates are heuristically assigned to the original and the downsized design based on their slack time determined by static timing analysis. Other gates are subjected to the genetic algorithm to perform an optimal downsizing assignment taking into account the previous assignments. The algorithm is applied for different downsizing factors to determine the optimal dual size for low energy operation without a performance degradation. Experimental results are obtained for some ISCAS-85 benchmark circuits such as 74283, 74L85, ALU74181, and 16 bit ripple carry adder. The proposed design shows an energy per cycle saving ranged from (29.6% to 56.59%) depending on the utilization of available slack time from the off-critical paths.

Keywords: Sub-threshold CMOS circuits, Dual size design, Slack based GA, Ultra low energy, Static timing analysis.

1. Introduction

Ultra low power consumption with medium frequency of operation (tens to hundreds of MHz) is the primary requirement for many applications such as portable computing gadgets or medical electronics. Hence, the operation with lower supply voltage may be more suitable way for power reduction in such applications,

Nomenclatures

DH	The high delay value of a gate at the downsizing factor *Kz*
DL	The low delay value of a gate at the original size
Kz	The downsizing factor
L	Transistor length
N	Total number of gates or nodes
slk	Gate slack time
SL	The lower limit of gate slack
SU	The upper limit of gate slack
T	Critical path delay
Vdd_{opt}	Optimal supply voltage for low energy operation
W	Transistor width

Greek Symbols

α	Switching activity factor.
β_1& β_2	The weighting coefficients of the objective functions, Eq. (5)

Abbreviations

DAG	Directed Acyclic Graph
EPC	Energy Per Cycle
PDC	Power-Delay-Capacitance Library
SBGA	Slack Based Genetic Algorithm
STA	Static Timing Analysis

whereas other traditional power minimization technique may be not efficient. For these applications the sub-threshold circuit design has been investigated [1-3]. The logic operations of sub-threshold devices are performed using the sub-threshold leakage current where this mode of operation is defined as weak inversion operation due to the lower supply voltage by Garett and Brattain in their Metal- Insulator-Semiconductor diode study [4]. Hence, operation in this region results in static and dynamic power reduction with the presence of performance degradation due to the expense delay which increases exponentially with the supply voltage reduction [5].

Leakage current integrates over effective delay period until leakage energy per operation exceeds the active energy. Hence, it is worth to developing models that investigate and illustrating the optimal supply voltage and design parameters for minimum energy point, and performance requirements [3].

Moreover, in sub-threshold circuits the energy per cycle (EPC) should be evaluated and used in the comparisons instead of the power where its value may be high even when power consumption is small because of the large delay. The approximate EPC of *N*-gates circuit is given in Eq. (1) [5, 6].

$$\text{EPC} = \sum_{i=1}^{N} 0.5\ \alpha(i).C(i).Vdd^2 + P_{leak}\ (i)\ .T \quad (1)$$

where *α (i)* is the switching activity of the i^{th} node, *C(i)* is the capacitance of the i^{th} gate, $P_{leak}(i)$ is the leakage power of the i^{th} gate and *T* is the critical path delay.

The 1st term of Eq. (1) represents the dynamic energy consumption results from the charging and discharging of gate load capacitance *C(i)* during the switching of the

circuit. The load capacitance appears at the output of each gate depends on the gate capacitance, fan-out of the gate, and wiring capacitances. The switching factor of a node represent the transition probability at which the node switches from 0 to 1 and consequently load capacitance is charging. The 2nd term represents the static or leakage energy which directly related to the leakage power and the critical path delay. This delay represent the largest path delay between the primary inputs and the primary outputs which determines the operation frequency of the circuit

2. The Related Work

In this section, the most important and related works for energy minimization and design methods in sub-threshold circuits are presented.

2.1. Sizing based techniques

The sizing of transistors is a well-known tool have been explored previously by many on super-threshold circuits. However, no such focus has been given to sub-threshold circuits [3]. However, transistor sizing is used in different ways to optimize the operation of sub-threshold devices through the optimization of the time delay of the device or the optimization of currents.

In [7], it has been theoretically shown that the minimum sized devices are optimal for energy minimization in sub-threshold circuits through the slightly increasing of supply voltage in order to balance the voltage transitions at the output of the gate.

The authors of [8, 10] demonstrated that the minimum size design is not suitable for fixed operation voltage applicationits and it is required to upsize the sub-threshold device in order to avoid parameter variability effects. Some transistor sizing guidelines were proposed in [8] for a higher functional yield, taking process variations into account. Moreover, it has been shown that minimum size devices are not always the best in terms of energy consumption in the sub-threshold region [9, 10] and the performance-driven stacked transistor sizing methodology has to be reconsidered [10, 11].

An optimized design for two 40 nm sub-threshold cell library was proposed in [12] to achieve robust operation at sub-threshold region with improved timing, area, and energy c/cs. This design was obtained through transition based transistor sizing technique to improve the worst rise and fall times by compromising the best rise and fall times.

In [13], a transistor sizing framework was proposed to find the optimum PMOS/NMOS transistor width ratio that maximizes the operation frequency without energy cost in sub-threshold circuits. Three mechanisms were used to obtain the optimal ratio of transistors width. These mechanisms were the largest current to capacitance ratio, delay minimization analytical approach, and the simulations of a ring oscillator in sub-threshold region.

In [14], transistor sizing and multi-threshold approaches were incorporated for sub-threshold flip-flop yield optimization in 65 nm and 28 nm CMOS technologies. The reliability and the energy of the new design was enhanced at the nominal temperature and power supply condition and in the worst-case.

In [15], a transistor sizing was proposed for an unbalanced logic cell design which proposed for sub-threshold biomedical applications. The unbalanced pull-up/down network design, inverse narrow width (INW), and the logical effort were exploited for better energy-efficiency and enhanced process variations.

The author of [16], derived a design guidelines for sub-threshold standard cell libraries. The low operation voltage was achieved through different approaches such as transistor sizing and body biasing with the effect of transistor staking.

However, all researches describe above focused on individual gates sizing for cell design. This can be considered as an ad-hoc design for energy minimization and performance requirements of a complete sub-threshold logic circuit.

2.2. Other techniques

The investigation of dual-vdd technique was presented in different works [17 - 20]. In [17, 18], the authors proposed a dual-vdd energy minimization methodology sub-threshold circuits. A mixed integer linear program (MILP) was developed to cancel the level converters need and to optimally assign the dual sub-threshold supply voltages at the maximum allowable frequency. In [10], the dual-vdd design was performed with a gate slack based algorithm to reduce the MILP complexity. The same problem of energy minimization with dual-vdd without level converters was studied in [20]. The authors proposed multiple logic-level gates to be used in the dual-vdd design. However, these technique requires additional supply voltages and show limited energy saving on an average of (8.2%) especially for the circuits in which the two voltages comparable and near *Vddopt* of the original design. The maximum energy saving (23.6%) was obtained with the case of 16 bit RCA at (0.21 V and 0.14 V) supply voltages.

The well-known dual threshold technique was investigated for energy minimization in 32 nm sub-threshold circuits [21]. A framework was proposed to assign the optimal reverse body bias for some gate of the off-critical paths to maintain the performance. However, this technique, is a threshold voltage based approach which has a significant drawbacks such as the requirements of additional supply voltages the threshold variation problems and the layout cost. Moreover, only active energy was minimized and limited by the increasing of bulk and tunneling currents where a maximum energy saving of (29%) was obtained for 32 bit RCA at 32 nm technology.

3. Circuit Model

The circuits to be optimized should be represented by a suitable model to fit the simulation requirements of the proposed methodology. This modelling can be achieved through the power-delay-capacitance (PDC) library generation, directed acyclic graph (DAG) representation, and the switching activity estimation. The static timing analysis is performed based on the DAG analysis and the contents of the PDC library as described later.

3.1. Library generation

All gates should be designed with different scaling factors in order to examine all possible sizes and then find the optimal size to be used with the original one in the dual size design. The width (W) of NMOS and PMOS transistors is used as $5L$ and

12*L* respectively, where *(L)* is the channel length which equal to the minimum scale. The downsized versions are designed with different scaling factors ranges from (*Kz*=0.9) to (*Kz*=0.2). The resultant width is (*Wz*=*W***Kz*) where the original width is obtained when (*Kz*=1) and the downsized widths is obtained when (*Kz* < 1).The second step in this library preparation is to classify the logic gates of the circuit according to gate type and no. of inputs such as (AND2, AND3, AND4, OR2, etc.). All these gates are considered with different fan-outs to cover all cases in the circuit. HSPICE is used with MATLAB interface to perform an accurate simulation for each gate type in order to obtain a power-delay-capacitance (PDC) library for all gates as shown in Fig. 1.

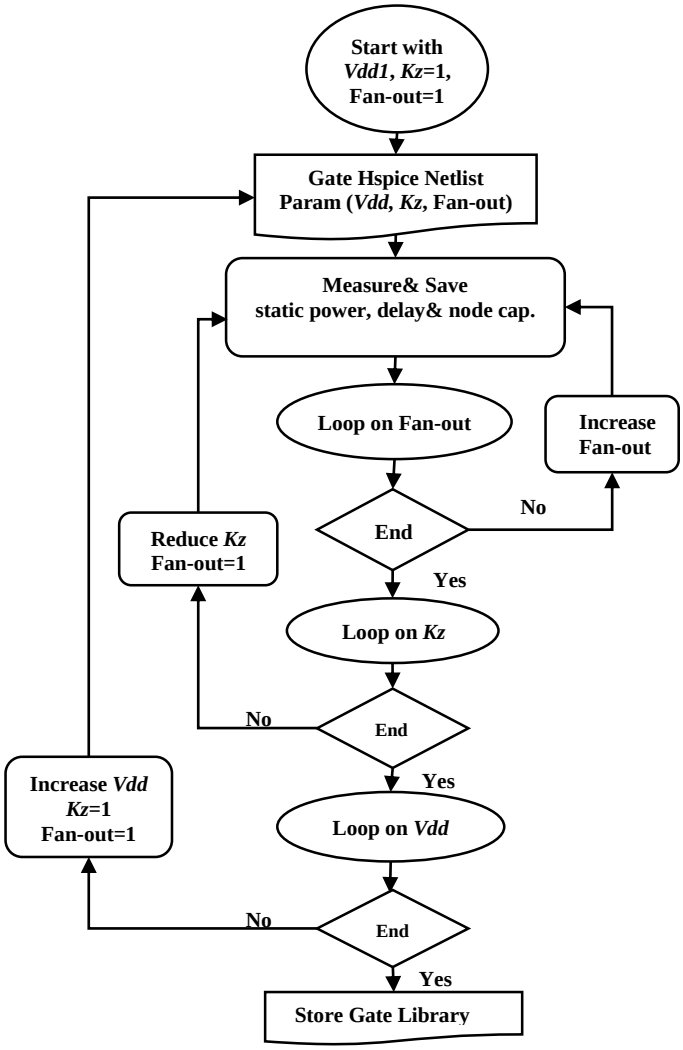


Fig. 1. Flow chart of PDC Library of each gate.

The library contains leakage power as a function of (*Vdd* and size), gate delay as a function of (*Vdd*, size, and fan-out or node capacitance), and node capacitance as a function of (*Vdd*, size, and fan-out). The assignment algorithm depends on the

library contents at each *Vdd* and size values to calculate and compare the overall power and delay.

3.2. Static timing analysis and switching activity estimation

The combinational circuit is represented as directed acyclic graph (DAG),G= (V, E). The logic gates represented as nodes or vertices within a set (V) whereas the connections between nodes are represented as a set (E) of directed edges from the inputs to the outputs. The first node is used to the represent the primary input and the last node used for the primary output.

Generally, the actual arrival time and required arrival time at the output of the gates are evaluated through the use of static timing analysis (STA). Moreover, STA is used to calculate the critical path delay (T) of the circuit and the slack time of each gate (slk). The gate slack is characterized as the difference between the critical path delay and the greatest path delay through this gate [6].

In this paper, the (All paths and cycle) Algorithm proposed in [22] is used to find all possible paths between any two nodes in a given DAG. Hence, by using the delay contents of the PDC library one can find the arrival time of each node, critical path delay and the slack of each node, as in the STA algorithm given in Table 1.

Table 1. STA algorithm.

1	Input: directed graph G =(V, E) and PDC library: where V is set of circuit nodes V=$\{v_1, v_2, \ldots . v_N\}$
2	Output: T: Critical Path delay and slk: slack of each gate
3	$\forall$ node $v \in V$ find:
4	gpi{v}=AP(G,1,v); all paths from node 1 to node v
5	gpo{v}=AP(G,v,N); all paths from node v to node N
6	D(v); delay of node v
7	D(v); delay of node v
8	TPI (v) ; the longest time from node 1 to node v,
9	TPO (v) ; the longest time from node v to node N
10	DP(v)=DPI(v)+TPO(v)+D(v); the longest path through node v
11	T= max{ DP(v) } where $v = 1 \sim N$; critical path delay
12	slk (v)=T- DP(v); slack of each gate

All paths from node (1) (primary inputs node) to any node (v) are given in Step 4 of Table 1. These paths are represented by the indices of nodes along each path. For each gate, the lower delay (DL) is obtained with the original size design (Kz=1), whereas the higher delay value (DH) occurs with specific lower size i.e. $Kz \neq 1$ for a given *Vdd* and fan-out values. Depending on these values the static timing analysis is performed at the specific supply voltage. After substituting the delay of each node from PDC library which may be DL or DH according to the algorithm assignments, the maximum delay from node (1) to node (v) is obtained. Similarly, the maximum delay from node (v) to node (N) (which is the primary outputs node) is determined in step 9. In step 10 the longest path through each gate is calculated depending on the previous results. The critical path delay of the overall circuit and the slack of each gate are calculated in steps 11 and 12 respectively.

Finally, it is required to estimate the switching activity at each node to complete the circuit model in order to evaluate and compare the EPC according to Eq. (1). Probabilistic estimation is used with the help of DAG analysis to evaluate the switching activity at each node, where the roots of the inputs for each gate can be determined.

4. Proposed Dual Size Design

As given in the previous section, each gate is designed with the original size transistors (with Kz=1) and with downsized transistors (Kz<1). The PDC library is evaluated for all gates under different values of fan-out, Kz and supply voltage (as shown in Fig. 1). Then the SBGA shown in Fig. 2 is automatically assign the original size design (Kz=1) to critical paths gates to maintain the performance. Consequently, the SBGA also finds an optimal set of gates on the off-critical paths that can be assigned to the downsized design (Kz<1) design without any performance degradation. For a given *Vdd*, the algorithm starts with the first downsizing factor (Kz= Kzj =0.9) and then the process is repeated for all other downsizing factors. The lower and upper values of the delay, static power and capacitance of each gate are determined as follows:

- DL(v): lower bound of gate delay, which occurs at Kz=1
- DH(v) higher bound of gate delay, which occurs at Kz<1
- PL(v): lower bound of gate power, which occurs at the Kz<1
- PH(v): higher bound of gate power, which occurs at Kz=1
- CL(v): lower bound of gate capacitance, which occurs at Kz<1
- CH(v): higher bound of gate capacitance, which occurs Kz=1

The assignment procedure can be described as follows:

Step1: The original gate design (Kz=1) is assigned for all gates so that the delay of any node D (v) will be DL (v). Then, the STA algorithm given in Table 1 is applied to find the critical path delay (T) and the slack of each gate slk (v). The critical path delay of this design at the specified *Vdd* is used as the timing requirement for the dual size design.

Step2: The downsized (Kz=Kzj) design is assigned for all gates so that the delay of any node D (v) will be DH (v). STA algorithm is applied again to find the new critical path delay (T_high) and delta value for each gate Δ (v) which equal to DH(v)-DL(v). The upper and lower slack bounds used in the optimization are calculated as, SU= (k-1).T/k and SL=min {Δ(v)} respectively where k = T_high/T.

Step 3: The first assignment process is given here. All gates have a slack time lower than the slack lower bound (SL) should be kept on the original size design (Kz=1) in order to keep the performance same as the original for the specific *Vdd*. These nodes are grouped in one set {Low_Set}. When any gate contained in {Low_Set} is switched from the original size to the downsized design, the delay of this gate is converted from DL to DH. Therefore gate slack will become negative as illustrated below in Eq. (2). However, the proposed assignment algorithm prevents this case because negative gate slack means a performance degradation occurred, where longest path delay exceeds the original circuit delay T.

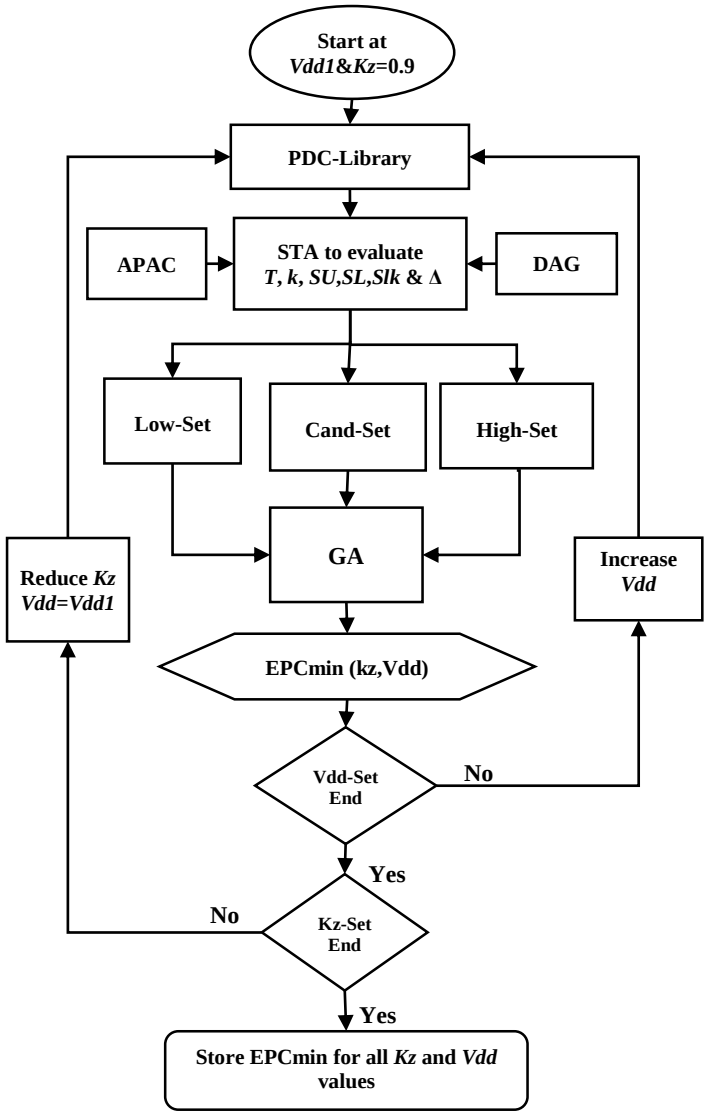


Fig. 2. The slack based genetic algorithm.

Step 4: The second assignment round starts at this step. All gates have a large slack time greater than the slack upper bound (*SU*) are switched directly to downsized design (*Kz =Kzj*) without any effect on the critical path delay. All these nodes are contained in a set called {High_Set}. The characteristic of this set is to have nodes with assignment properties still keep its slack non-negative, as illustrated below in Eq. (3) and Eq. (4).

Let us consider, *slk** (*v*) is the updated gate slack after the switching of gate (*v*) from original design to the downsized design. Consequently, *DP**(*v*) is used for the

updated longest path delay of gate (v) after gate downsizing assignment. For the gates with a gate slack (slk (v) < SL),

$$slk^*(v) = T - DP^*(v) = T - [DP(v) + \Delta(v)] = slk(v) - \Delta(v) \quad (2)$$

Equation (2) will be negative since SL is defined to be: slk (v) < $SL \leq \Delta$ (v). As for the gates whose gate slack slk (v) ≥ SU,

$$slk^*(v) = T - DP^*(v) = T - \frac{T_{high}}{T}.DP(v) = T - \frac{T_{high}}{T}.[T - slk(v)] \quad (3)$$

From the definition of SU, it is known that slk (v) ≥ SU = (1-T/T_{high}) T,

$$T - \frac{T_{high}}{T}[T - slk(v)] \geq T - T_{high} + \frac{T_{high}}{T}SU = 0 \quad (4)$$

Therefore, the result of Eq. (3) remains non-negative after downsizing assignment. Here an approximation is used that $k = T\_high/T \simeq DP^*(v)/DP(v)$.

In above eq., T_{high} is the critical path delay after the downsizing of all gates. DP (v) and DP^*(v) are the longest path delay through gate v with ordinary and downsized versions respectively. The evaluation of these parameters is performed by using the static timing analysis as given in Table 1.

Step 5: The other nodes are not processed with the previous two sets; the nodes have slk (v) < Δ (v) which cannot be modified and therefore should be added to the first set {Low_Set}. Other nodes that have slk (v)> Δ (v) will be candidate for switching from the original size (Kz=1) to the small size ($Kz = Kzj$). These nodes are grouped in a new set {Cand_Set}. Some of the nodes contained in this set are optimally assigned to the downsized design through the application of the modified genetic algorithm.

Step 6: At this step, the genetic algorithm is performed. In the initialization process, the population size, crossover, and mutation probabilities are determined. The individual length should be the same as the number of nodes contained in {Cand_Set}. Binary encoding is used to represent the nodes in each individual. (0) is used for the original design assignment and (1) is used for the downsized design assignment.

The nodes in (Low-Set} should be assigned to (0) whereas nodes in {High-Set} should be assigned to (1). The node assignment in {Cand-set} is randomly generated in the first step. For each individual which represents the nodes of {Cand_set}, all above three sets are mixed according to their node indices in order to generate a full vector that represents nodes indices of the overall circuit. Depending on this vector and through the use of PDC library the corresponding EPC (Ex) is calculated according to Eq. (1). Also, the corresponding critical path delay (Tx) is evaluated, where STA algorithm is applied again. The delay of each node D (v), which may be DL (v) or DH (v), is determined according to the gate assignment in the final vector. These two objectives (Ex and Tx) are used to generate the fitness value as given in Eq. (5).

$$\text{fitness} = \beta_1 Ex + \beta_2 Tx = \beta_1\left(\sum_{i=1}^{N} 0.5\alpha(i).C(i).Vdd^2 + P_{leak}(i).Tx\right) + \beta_2 Tx \quad (5)$$

where β_1 and β_2 are the weighting coefficients of the energy and delay objectives, respectively. Their values representing the relative importance of the objective in the problem and the sum of β_1 and β_2 should be equal 1.

A new generation is obtained after the selection of the better 50% individuals, cross-over and mutation steps. The genetic algorithm steps are repeated until the minimum fitness value is obtained. As a result, the maximum delay after the dual size assignment does not exceed *T* (the critical path delay of the original circuit at the specific supply voltage) and the optimized EPC is determined. This process is repeated for all *Kz* values and the presented framework finds the optimal supply voltage (*Vddopt*) and the optimal downsizing factor that be used with the original value to perform the proposed dual size design.

5. Experimental Results and Discussions

In this section, a simulation details and experimental results of the proposed dual size design are given. The transistor model used is PTM 22 nm CMOS technology. The supply voltage used in the simulations ranges from 0.25 V to 0.4 V in steps of 0.01 V (i.e. 16 values of supply voltage are used), and the sizing scale *Kz* ranges from 0.2 to 1 in steps of 0.1.

Experimental results of the dual size design and the classical design are obtained and compared for some benchmark circuits (16bit RCA, 74L85, 74283 and ALU7418). The EPC simulations of these circuits are shown in Fig. 3, Fig. 5, Fig. 7, and Fig. 8 respectively. Table 2 gives more detailed analysis, where optimal EPC, *Vddopt*, *Kz*, *T*, and percentage of modified gates are given for all circuits. An assignment counter is used to count the number of the downsized gates during the assignment procedure. Hence, the percentage of the small gates is evaluated as (number of downsized gates/total number of gates)×100%. Also, the amount of EPC saving is evaluated from the comparison of the EPC of the dual size design with that of the original design as (1- new EPC/original EPC)×100%.

The amount of energy saving achieved by the dual size design is influenced by the circuit topology. The framework select one downsizing factor and apply the assignment algorithm for all possible values of *Vdd*. The algorithm selects some gates of the non-critical paths to be switched from the original design to the downsized design. Each sizing scale results in one curve when used with original size as shown in EPC figures and there is a minimum EPC at an optimal *Vdd*. The lowest energy occurs at *Vddopt* of the lowest energy curve, i.e. the optimal *Vdd*-optimal *Kz*.

Maximum energy saving (56.59%) is achieved for the 16 bit RCA at optimal *Kz* (0.2) and *Vddopt* (0.32 V) which corresponds to (9.915 nS) critical path delay. The 16 bit RCA circuit explores a large number of short off-critical paths and the path length difference between the critical path and off-critical paths is sufficiently large. This can be noted from the gate slack histogram of the non-optimized circuit shown in Fig. 4(a). The proposed framework try to select the best scale size that optimally utilize this available slack in such a way to reduce the EPC at the optimum *Vdd*. Therefore, this case allows more gates (64.58 % of total gates) to be assigned to the downsized design (*Kz* = 0.2). This assignment process reduces the available slack time in the optimized circuit as shown in Fig. 4(b). This is due to the delay increasing of the downsized gates.

Moreover, this methodology offers another benefit of area saving proportional to the assignment percentage and the sizing factor. Hence, this saving can be evaluated as: Area saving = (1-*Kz*) × Percentage of small gates.

For 16 bit RCA, the transistors of the downsized gates are scaled by a factor of 0.2 (i.e. 80% of gate area is saved). This results in (51.6% area saving) because of 64.58 % of the gates are assigned to the down-scaled design.

The well-known 4-bit magnitude comparator (74L85) circuit is characterized by the relatively balanced structure. The schematic, Verilog structural model, and other details of this circuit and all other circuits are found in [23]. This circuit shows the lower bound of energy saving (29.6%) at *Vddopt* (0.32 V). This is due to the large number of critical paths. Therefore, there are large number of candidate gates with small slack time and few gates with relatively large slack time as shown in Fig. 6(a). There are two main assignment options. The first is to assign large downsizing for the few number of gates that have enough slack time. The second option is to use moderate downsizing assigned to the large number of gates that have moderate and high slack time. This due to the inverse proportional relation between the gate delay and the scaling factor (*Kz*) value. The EPC of each case is evaluated and compared to select the best design option.

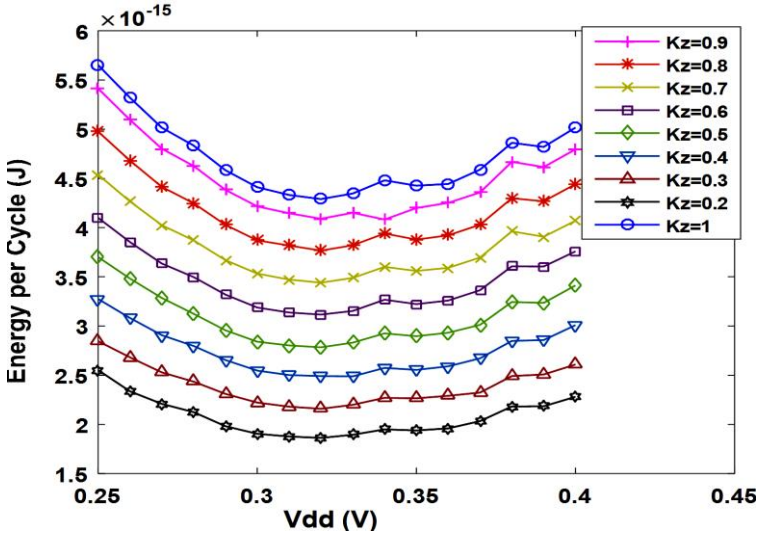
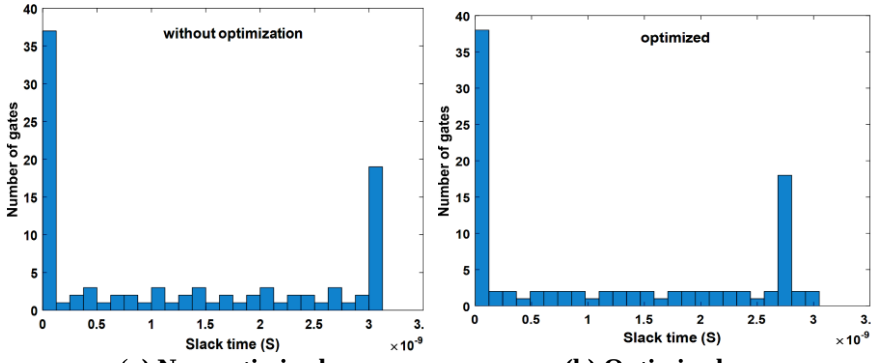


Fig. 3. EPC of 16 bit RCA circuit.



(a) Non-optimized. **(b) Optimized.**

Fig. 4. Slack time of 16 RCA at *Vdd*=0.32 V.

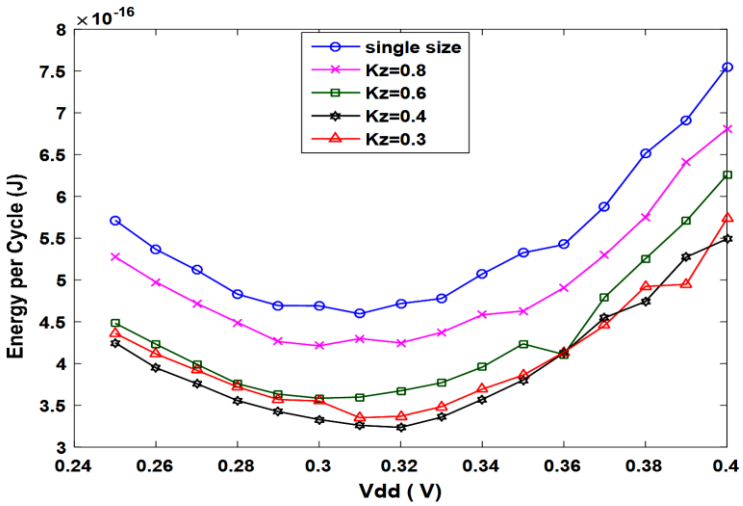
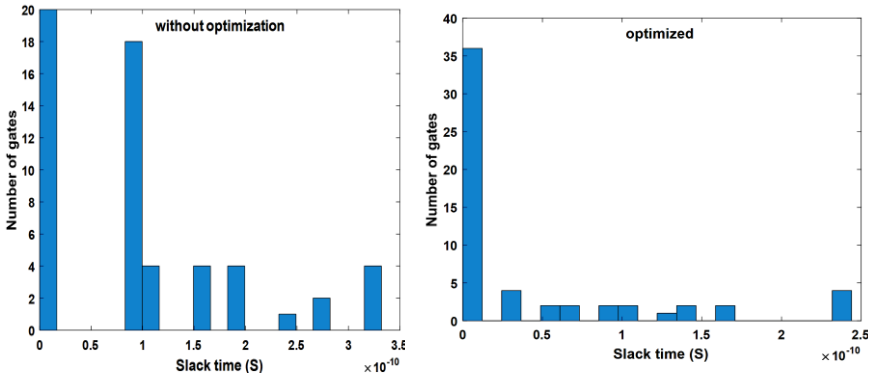


Fig. 5. EPC of 74L85 circuit.

As described above, the algorithm selected the downsizing factor (*Kz*=0.4) as an optimum case which considered suitable for all candidate gates. However, Kz of (0.4) will optimally exploit the available slack time as shown in Fig. 6(b) but the energy saving will be small as compared with other circuits.

Moreover, the area saving may be another benefit where 56.3% of gates is downsized by a factor of 0.4. Hence, the area saving obtained from this process is (33.81%).



(a) Non-optimized. **(b) Optimized.**

Fig. 6. Slack time of 74L58 at *Vdd*=0.32 V.

The other two circuits show EPC saving of (39.07% and 31.9 %) for 74283 and ALU74181 respectively as given in Table 2. This depends on the circuit topology and how can the downsizing algorithm exploit the available slack time of each circuit at the optimal supply voltage. The area saving of these circuits depends on the small gates assignment percentage. Hence, an area saving (42%) is obtained for 74283 due to 60% of gates are assigned to 0.3 scaling and 41.44% area saving is obtained for ALU74181 due to 59.2% of gates are assigned to 0.3 scaling also.

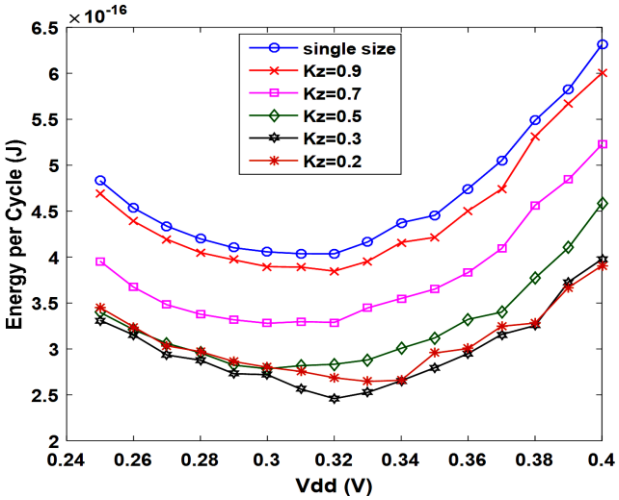


Fig. 7. EPC of 74283 circuit.

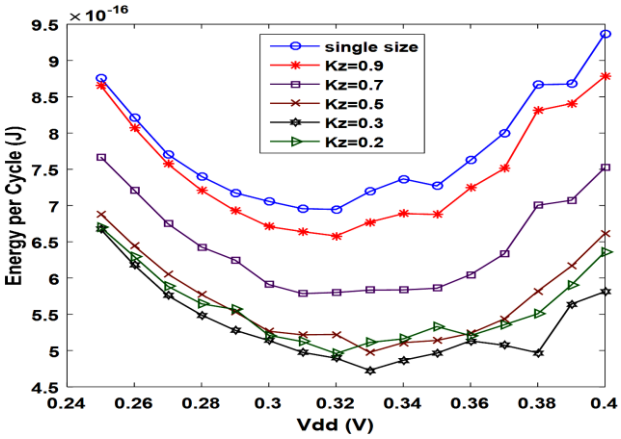


Fig. 8. EPC of ALU 74181 circuit.

Table 2. Experimental result of simulated circuits.

Circuit	Design	EPC (f J)	T ns	*Vdd* opt. (V)	*Kz* opt.	EPC Saving (%)	Small Gates (%)	Area Saving (%)
16 bit RCA	Single	4.290	9.915	0.32	-	-	-	-
	Dual	1.862	9.915	0.32	0.2	56.59	64.58	51.6
74283	Single	0.403	1.962	0.32	-	-	-	-
	Dual	0.245	1.962	0.32	0.3	39.07	60	42
ALU 74181	Single	0.694	2.424	0.32	-	-	-	-
	Dual	0.472	2.241	0.33	0.3	31.9	59.2	41.44
74L85	Single	0.459	2.50	0.31	-	-	-	-
	Dual	0.323	2.18	0.32	0.4	29.6	56.36	33.81

For another design aspect, the circuit can be designed with a power delay trade off according to the application requirements. Table 3 show samples of this trade-off for the 16bit RCA and 74L85 circuits at the optimum dual size design of each circuit. However, it can be noted from this table that the power dissipation reduce with the reduction of *Vdd* but this is not the case for the PDP. This is due to the large delay increasing with the reduction of *Vdd*. Hence, for sub-threshold circuits, the energy evaluation should be used in the comparisons in case of energy minimization issue.

Table 3. Power delay trade off for 16RCA and 74L85 circuits.

	16 RCA/*Kz*=0.2			**74L85/*Kz*=0.4**		
***Vdd*(V)**	**P(nW)**	**D(nS)**	**PDP(fJ)**	**P(nW)**	**D(nS)**	**PDP(fJ)**
0.25	96.89	26.33	2.552	69.690	6.08	0.424
0.27	115.14	19.17	2.208	85.499	4.38	0.375
0.29	137.79	14.37	1.981	105.84	3.23	0.342
0.31	168.64	11.13	1.877	130.29	2.50	0.326
0.32	187.79	9.915	1.862	147.69	2.18	0.323
0.33	208.01	9.105	1.894	168.42	1.98	0.335
0.35	257.57	7.52	1.938	230.72	1.64	0.38
0.37	318.15	6.39	2.033	332.60	1.36	0.454
0.39	393.72	5.54	2.184	433.74	1.21	0.527

6. Conclusions

This paper, presents an ultra-low energy dual size design for CMOS subthreshold circuits. Some gats of the circuit are optimally downsized using the proposed SBGA to reduce the EPC at the maximum allowable performance. A significant energy saving ranged from (29.6%) to (56.59%) is obtained depending on the circuits structure. Moreover, an area saving is obtained with the optimized circuit which proportional to the optimal downsizing scale and the number of gates. Hence, this area saving ranged from (33.8%) to (51.6%). As noted from the results, this technique improves the area and the energy efficiency of the design with less costs as compared with the threshold based and *vdd* based techniques. Moreover, this work presents a clear sizing design based on the conventional gate sizing and then minimize the energy. Hence, this strategy reduces the ad hoc design difficulties in terms of energy and performance requirements of subthreshold circuits.

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