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Proposed low Xilinx FPGA power consumption for recursive NOMA applied in optical visible light communication

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Abstract

Today the NOMA has exponential growth in the use of Optical Visible Light Communication (OVLC) due to good features such as high spectral efficiency, low BER, and flexibility. Moreover, it creates a huge demand for electronic devices with high-speed processing and data rates, which leads to more FPGA power consumption. Therefore; it is a big challenge for scientists and researchers today to recover this problem by reducing the FPGA power and size of the devices. The subject matter of this article is producing an algorithm model to reduce the power consumption of (Field Programmable Gate Array) FPGA used in the design of the Non-Orthogonal Multiple Access (NOMA) techniques applied in (OVLC) systems combined with a blue laser. However, The power consumption comes from Complex Digital Signal Processing (DSP) due to mathematical operations such as addition and multiplication which consume more FPGA power when compared with other parts of NOMA. The multiplication operation consumes more FPGA power than the additional operation. The article's goal is to propose low FPGA power consumption algorithms called recursive IFFT/FFT which reduce the FPGA power consumption by more than 45% compared with the model without the proposed algorithm using AMD Xilinx Kintex-7 with high-speed analogue card.

1. Introduction

Today, the exponential growth of wireless services such as mobile networks, underwater networks, Internet of Things IoT, and Internet of Underwater Things IoUT applications has created a huge demand for Broadband signal reception and processing. Therefore, the OVLC technology is based on a light that offers a high data rate and free spectrum. This technology was a great solution to broadband applications but still consumes more FPGA power due to the signal processing operations. The motivation is to reduce the FPGA power consumption for OVLC systems based on NOMA techniques. The most valuable resource in the network communication world is the processing of data applications [1]. Optical Wireless Communication (OWC) uses visible light as the carrier in the OWC system and the OVLC is a potential way to extend the limited communication performance of VLC by utilizing the communication capability of the blue uses laser diode LD. The spectrum of laser light in the peak area at about 450-470 nm; the blue LD spectrum generally has a wide spectrum and the emitted power is larger when compared with other colour LD light [2]. The blue LD has high output power, a large modulation bandwidth, and no coherence due to the thermal noise of the quantum effect like the laser, so the application of the LD has a higher advantage. At present, the blue laser LD has a very mature manufacturing technology, and the LD's emission efficiency has also become very high, productive, and low loss. Since the output power and industry of the LD have also become very mature and suitable, this paper uses blue laser LD as the lower layer of the system.

The optical laser OVLC is the promising technology to replace the traditional data transfer technology which depends on traditional wireless communications [3]. The (LD) is a main component of the transmitter and receiver used indoors and outdoors for different environments such as space and underwater and offers high transmission capability with free spectrum when compared with traditional wireless communications [4]. Therefore, the VLC technology was attracting interest from both academic researchers and industrial manufacturing sectors [5]. Non-orthogonal multiple access has been recognized as a promising solution for the next-generation network and beyond wireless communication systems because of its excellent ability to increase the number of connected terminal devices. The NOMA is capable of occupying the same spectrum resources at the same time and the same frequency for multiple terminal devices, and sharing the same optical power. Compared to the mainstream orthogonal multiple access technology, it has the characteristics of high-frequency utilization efficiency, great potential in increasing the number of connected terminal devices, and high security. Inevitably, the non-orthogonal feature of NOMA causes inter-channel interference occurrence, which needs a scheme that gives the system the ability to mitigate the interference. Remarkably, the fractionally spaced decision feedback recursive orthogonal frequency division multiplexing system is employed in a NOMA optical wireless communication system for optical visible light communication to solve the inter-channel interference issue caused by single-carrier NOMA because of its sensitivity to interference, thereby improving the transmission quality. It is well known that optical intensity modulation and direct detection systems have large signal-to-noise ratios (SNRs) and large bit error rates (BERs) due to Shot Noise and thermal noise. To reduce the SNRs and BERs, we used multi-carriers for one subscriber. Multiple carriers can be generated by a digital signal processor and their phases and amplitudes can be controlled.

However, various strategies have been proposed for OVLC transmission to increase the communication capacity but this will lead to an increase in FPGA power consumption due to an increase in the DSP [6, 7]. Therefore, the FPGA power consumption is an important factor that will be used in the next generation networks and OVLC systems with NOMA as a base modulation [8]. There are some parameter effects on the FPGA power for NOMA modulation such as the bit precision, twiddle factor, length, and mathematical algorithms of IFFT/FFT such as Cooley- Tukey algorithms with implementation engine type such as pipelined-streaming I/O, Radix [9, 10]. Therefore, the scientist targeted a power reduction technique for green network communication [11]. The applications with hungry bandwidth and power consumption such as cloud computing, IOT applications for space and IOUT underwater [12, 13], and high-resolution video [14,15]. In addition, there are many methods used to reduce power consumption some of them are used to control the length of FFT/IFFT to get the same data rate with short length FFT/IFFT this will lead to reducing the FPGA area and reduce the power consumption [16, 17]. The most FPGA power consumption is coming from Complex (DSP) because of the mathematical operation inside IFFT/FFT to do the Subcarriers orthogonality of the subcarriers between them. Therefore, reducing the DSP processing by reducing the length, precision, and algorithm type of IFFT/FFT will lead to reducing the FPGA power [18]. The state-of-the-art of this paper is producing a new IFFT/FFT recursive algorithm that consumes low FPGA power. However, many previous study methods to perform the algorithms of recursive FFT/IFFT such as Goetzel's algorithm, Yang and Chen, and Clenshaw algorithm [19]. All those recursive FFT/IFFT algorithms focus on reducing the mathematical operation and complexity. Therefore, this research paper proposes a new recursive algorithm that reduces the power consumption in FPGA by using recursive IFFT when compared with a traditional method that uses IFFT/FFT to generate the NOMA symbol. The objective of this algorithm is to reduce the mathematical complex operation applied in the OVLC system. The approach is reduced by the multiplication mathematical operation and replaced by the addition mathematical operation [20]. As we know, the mathematical additional operation consumes lower FPGA power when compared with the multiplication mathematical operation. The main contribution of the research is to reduce the FPGA power consumption by proposing an algorithm of IFFT/FFT that consumes lower FPGA power when compared with other algorithms used in NOMA for multiplexing the subcarriers. In addition, using AMD Xilinx evaluation board Kintex-7 with a high-speed analogue card called KC705-325T from Avent. This type of card can estimate FPGA power consumption in the stage of pre-design and pre-implementation in cooperation with MATLAB using a system generator and Simulink for the design. The power estimation data file(.xpe) generated from the ISE 14.7 design after simulating the design this file was imported by Excel spreadsheet to estimate the FPGA Power.

Finally; this article presents an estimation power consumption method of the proposed algorithm applied in the design of IFFT/FFT using special tools from AMD Xilinx which is named XPower estimation tool.

2. Research Methodology

NOMA is a promising modulation technique used in optical VLC systems using laser. The main goal is to reduce power consumption when increasing network bandwidth capacity. This power comes from Complex digital signal processing and mathematical operations. The complex IFFT/FFT uses a Cooley-Tukey algorithm with a Radix2 butterfly processing engine [21, 22]. The mathematical equation described in equation (1) below:

$$X(n) = \frac{1}{N}\sum_{n=0}^{N-1} x_{(k)}\, e^{-j2\pi\frac{nk}{N}} \qquad (1)$$

where X(n): Time domain, X(k): Frequency domain, N: length FFT, K: 0...N-1.

In VLC networks NOMA is the best modulation technique [23, 24]. The proposed method uses recursive IFFT instead of regular IFFT which reduces the mathematical multiplication processing operation and is replaced by an additional operation which leads to a reduction in the power consumption of FPGA. The numbers of addition operations inside recursive IFFT are increased when compared with the number of multiplications. The mathematical operation equations (2) describe the previous recursive algorithm.

$$H_k^{previous} = \sum_{n=a-(N-1)-1}^{a-1} x_{(n)}\, e^{-j2\pi\frac{nk}{N}} \qquad (2)$$

K: FFT/IFFT bin number.

$$H_k^{now} = H_k^{previous} + x_a\, e^{-j2\pi\frac{ak}{N}} - x_a - Ne^{-j2\pi\frac{ak}{N}} \qquad (3)$$

where $\mathbf{H_k^{now}}$ recursive FFT output. x_a current sample.

Equation (3) represents the proposed recursive IFFT using an addition operation to do the orthogonality between subcarriers and generate the NOMA signal. The number $e^{-j2\pi\frac{ak}{N}}$ are the power of the N^{th} root of unity and are normally stored in a look-up table. The design of an adaptive digital filter that is implemented inside the IFFT/FFT is shown in Figure. 1.

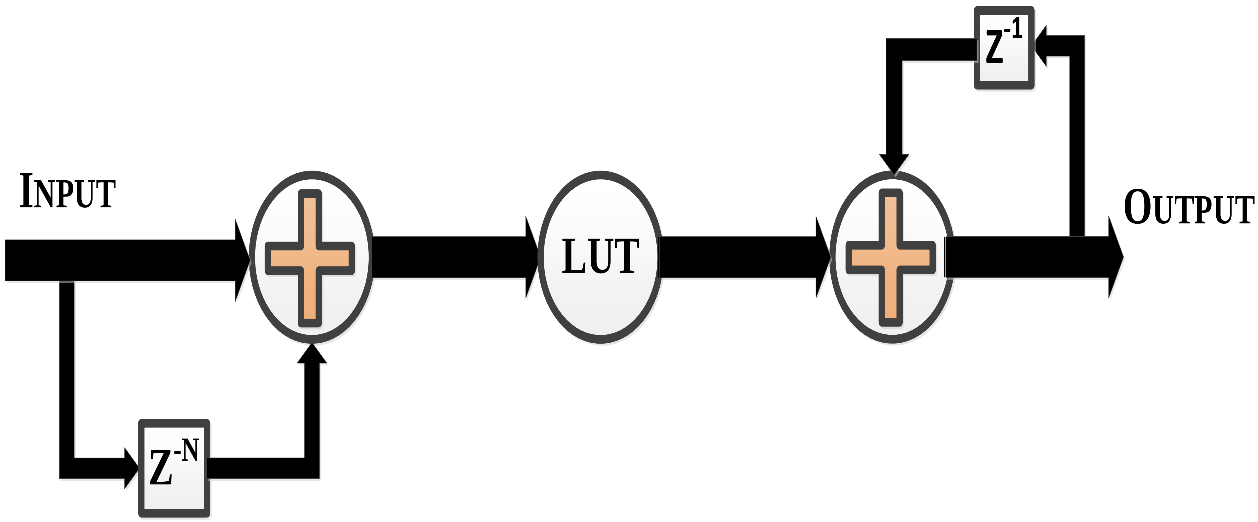

Fig. 1. NOMA Recursive FFT/IFFT component diagram.

In the figure above the main component to construct the IFFT/FFT. However; the operation procedure is the input subcarriers are added with delay N which is the IFFT length. The output result is stored in the Look-Up Table (LUT). The data stored in LUT is added to the output IFFT with one delay called the previous output. The result from this part is the recursive NOMA symbol which is used in the OVLC system.

The estimated FPGA consumption power procedure of the recursive and complex NOMA system transceiver model is explained in this part. The design uses special tools supported by MATLAB and Xilinx to estimate the thermal specification and power of FPGA during any phase in the design cycle. This tool provides analyses and thermal power consumption in detail. The implementation uses a Xilinx KC705 evaluation board with high-speed analog designed by Avnet [25]. In the design phase, AMD Xilinx provides a Simulink tool cooperated with MATLAB system generator and using Xilinx (Integrated Synthesis Environment) ISE-14.7. This experiment uses modulation type Quadrature Phase Shift Keying (QPSK) with symbol rate 30.72 M Symbol/Sec with 256 points length of IFFT/FFT length. The program is set to get the power estimation during the design cycle system generator Simulink block.

The first steps start from board type definition in this design project using the AMD Xilinx system-generator block type Kintex-7 /XC705-325T-2 /ffg900. After that, the report of power is generated by the model design. The generated report includes hierarchy, total, and thermal power. The XPower analyzer report includes supply voltage, functional logic, and static and dynamic power.

The Excel spreadsheet was designed by AMD Xilinx and is used to estimate the FPGA power of each part of the model in the pre-design and pre-implementation phases of the project when designed in the ISE design suite and the Vivado power analyses. The data is imported from the design to the Excel spreadsheet by clicking the import file as described in Figure (2). The advanced power report generated is used in the next section to represent and analyze the estimation power as a graph for components as functional of on-chip power as a variation of each function block, variation of power with core voltage, junction temperature, and static and dynamic power.

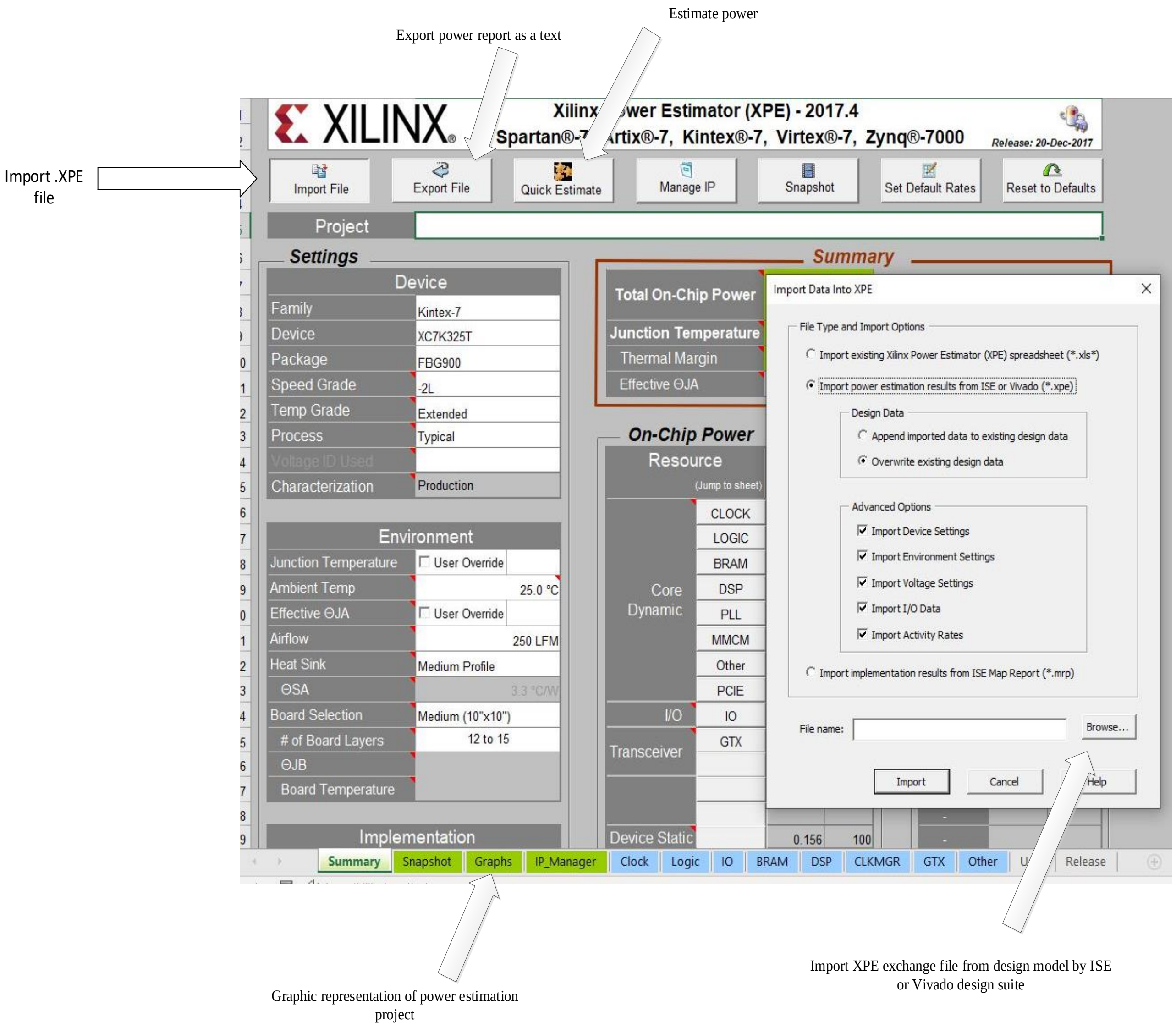

Fig. 2. General estimation power Excel spreadsheet.

The next section discusses the result and compares the FPGA consumption power of two NOMA design systems using complex IFFT/FFT, with the other proposed method using Recursive IFFT/FFT with low FPGA power consumption used in optical wireless communications.

2.1 Optical NOMA system by complex FFT/IFFT

This section explores the power consumption analyses by implementing 8-bit precision, QPSK modulation with a bit rate of 61.44 Mb/Sec and 256 points IFFT/FFT length. The IFFT/FFT type is used as a logic core IP V.8 implemented by the Cooley-Tukey algorithm. The I/O architecture is Pipeline streaming IO with a radix2 butterfly processing engine. The main block diagram of the VLC system used complex NOMA shown in Figure. 3.

The block diagram of the VLC system starts from modulation and then multiplexed the signal by using complex IFFT to generate subcarriers multiplexing. The cyclic prefix was added to prevent inter-symbol interference. The signal generated is converted to analog by a DAC converter. After that, add DC bias to the analog NOMA signal then move to the LED to transmit the NOMA signal over the VLC channel. On the receiver side, a photodiode receives the NOMA signal after removing the DC bias and then demodulates to get the original data.

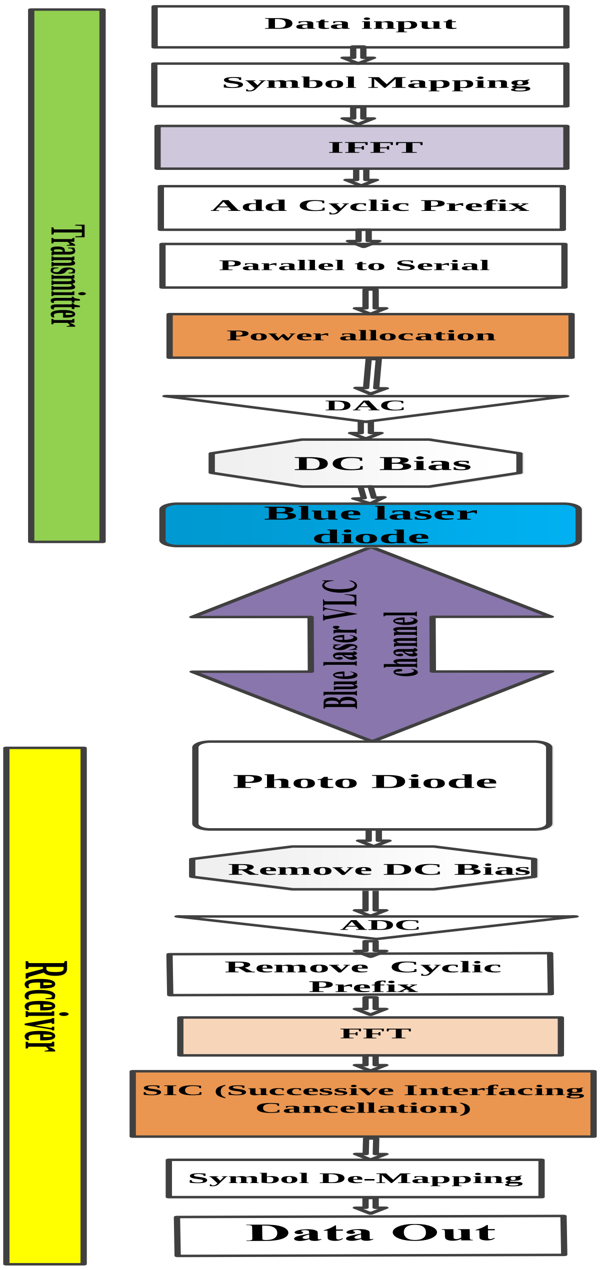

Fig. 3. Flow chart NOMA of VLC system by Complex IFFT/FFT.

2.2 Optical NOMA system by Recursive IFFT/FFT

OVLC is used for high-data-rate and wide bandwidth applications; the modulation types use a multicarrier NOMA as a main modulation technique because of flexibility [26]. Therefore, the best solution to find the FPGA power consumption by use Recursive IFFT/FFT instead of Complex (IFFT/FFT). As we know the multiplication operation consumes more FPGA power when compared with the mathematical additional operation [27, 28]. This system has used an algorithm to compute IFFT/FFT by reducing the mathematical multiplication operation and increasing the additional operation [29,30]. The output result from recursive IFFT is the multiplexed NOMA subcarriers. The orthogonal signal is transmitted to DAC/ADC and connected to the board Kintex-7 through the FMC connection terminal, with a sampling rate of 245.76MS/Sec. After converting the signal to analog by convertor, add DC bias and transmit the signal through the blue laser diode to transmit through the VLC channel. The received signal through the laser photo-diode then removes the DC bias and converts the signal through the ADC. Finally, the signal is DE-multiplexed through recursive FFT to create the original signal. To represent the process above as a simple flow chart block diagram as in Figure. 4.

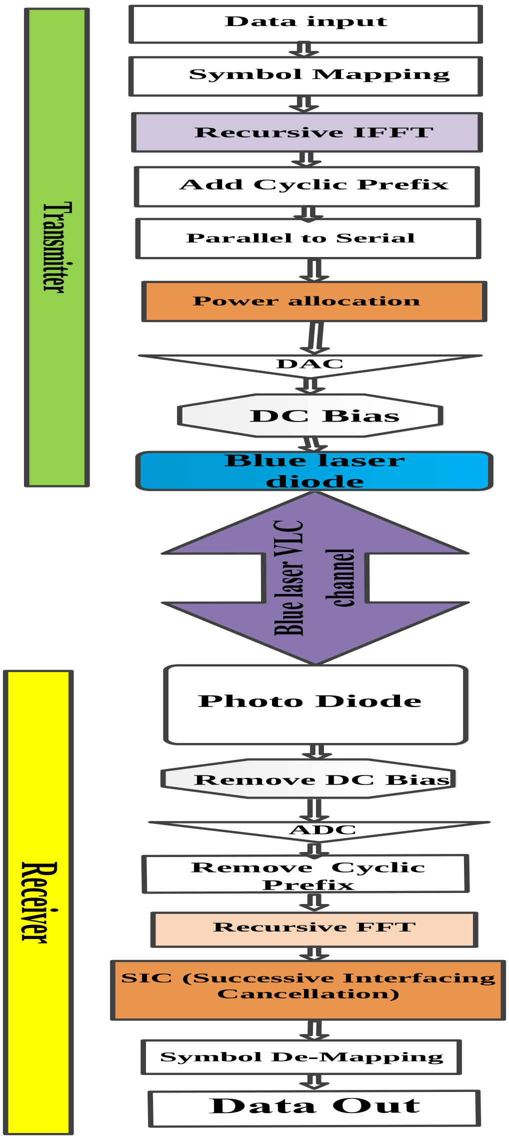

Fig. 4. Flow chart of optical NOMA system by Recursive IFFT/FFT.

3. Results and Discussion

The result of optical NOMA with complex IFFT/FFT shows that the IFFT/FFT power consumption is higher than that of the other AMD Xilinx block in the design, which consumes 12.18mw/12.28mw. When compared with another part of the OVLC system, the XPE file generated from the ISE is an XPower analyzer used in the Excel spreadsheet to estimate consumption power, as in Table 1.

Table 1: Power Estimation of NOMA with Complex IFFT.

Resources		Power (W)
Dynamic	Clock	0.045
	Logic	0.007
	BRAM	0.02
	DSP	0.006
	I/O	0.018
Static		0.159
Total power		0.255

The relationship between junction temperature and power consumption can be represented in Figure. 5. The relationship shows that increasing the estimation power will lead to an increase in the junction temperature of on-chip power at a typical 1V. However, the result shows a forward relation between junction temperature and total and static power of the on-chip.

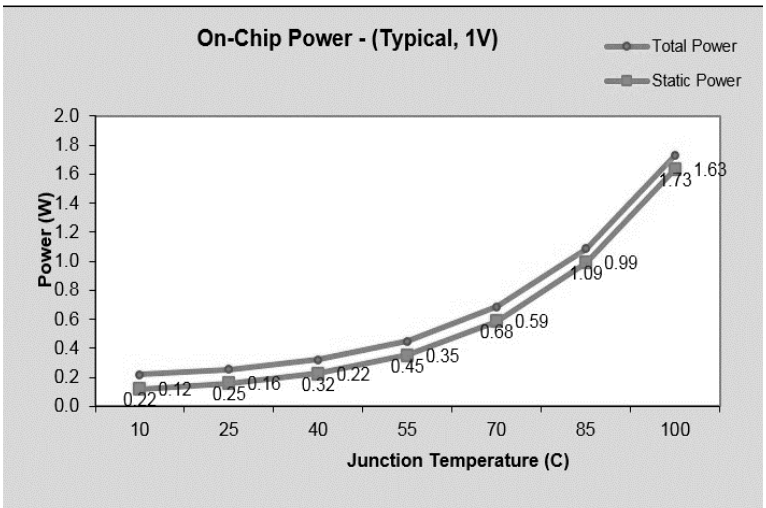

Fig. 5. Power and junction temperature of Complex NOMA.

The result of the proposed model for optical NOMA with an estimation of power consumption generated after implementation in the system generator. The XPE file is generated from the power analyzer report as in Table 2 In the Xilinx, Excel spreadsheet represents the power of each logic component by graph.

Table 2: Optical Recursive NOMA Power consumption

Resources		Power (W)
Dynamic	Clock	0.045
	Logic	0.007
	BRAM	0.02
	DSP	0.006
	I/O	0.018
Static		0.159
Total power		0.224

The junction temperature of the VLC system using a complex OFDM design model includes IFFT/FFT as in Figure. 6. The power consumption on junction temperature is decreased when compared with the previous experiment.

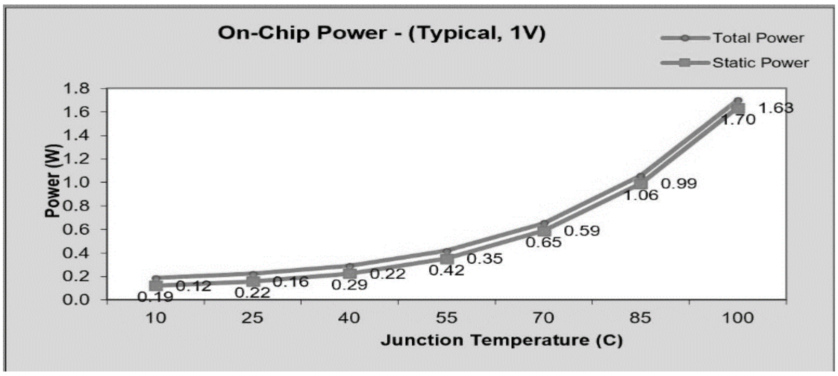

Fig. 4. Junction Temperature with power consumption recursive NOMA.

Compare it with the result in Table 1. The (on-chip power) 0.255W and 0.224W show a reduction in total NOMA system power. When comparing the result by using ISE14.7 of the complex and proposed models used in OVLC by NOMA techniques as shown in Figure. 7 and 8. Which represents the FPGA power report of each part of the model design.

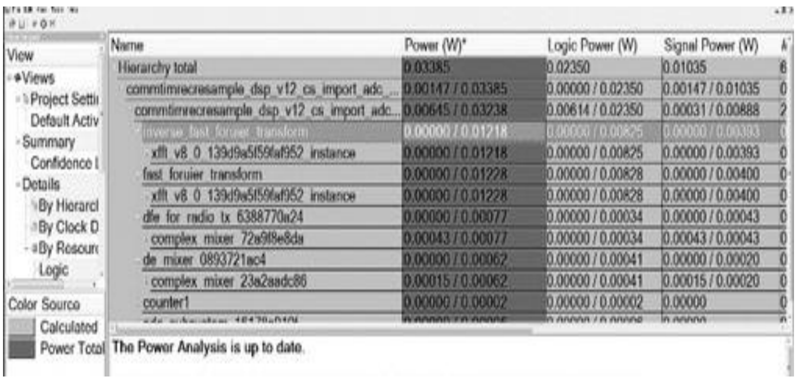

Fig. 7. Power consumption of complex IFFT/FFT.

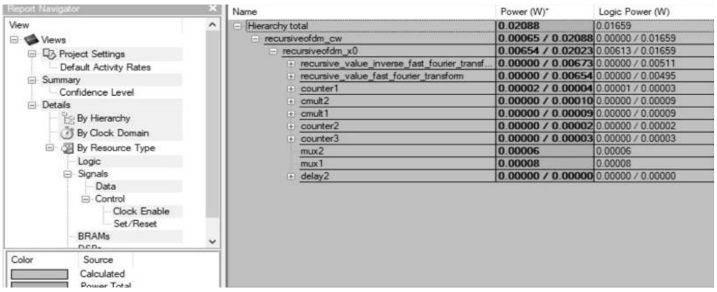

Fig. 8. Power consumption of proposed recursive IFFT/FFT.

The result above shows the FPGA power consumption of the OVLC system using Recursive FFT/IFFT is reduced by more than 45% when compared with complex IFFT/FFT. The power consumption of recursive IFFT is 6.73 mW compared to 12.18 mW when using traditional complex IFFT. The power consumption was analyzed by using an Excel spreadsheet from Xilinx.

The results shown in Tables (1 and 2) show that the FPGA power consumed by the clock reduced from (0.045 to 0.025) W which means reduced by 45%. The Logic component's power was reduced from (0.007 to 0.005) which means reduced by 29%. BRAM is reduced from (0.02 to 0.018) which means a 10% reduction. The DSP power shows that a reduction (0.006 to 0.005) W means a 17% reduction in processing. finally, the (I/O) power is reduced from (0.015 to 0.012) W. All components were reduced in power for the proposed model in this paper which means a good feature for future OVLC network communications when using NOMA techniques.

4. Conclusions

The FPGA power consumption is crucial for future next-generation optical VLC which uses blue Laser light as an important component with NOMA modulation. Therefore, FPGA power consumption is a critical challenge for future network components. The main goal is, to reduce the FPGA power consumption in the OVLC system. The above experiments comparing two modulation types have used the algorithm of Complex NOMA and Re-cursive NOMA with the blue laser VLC system. The practical significance of this paper produces a low FPGA power consumption algorithm called recursive FFT/IFFT which is applied in the blue laser NOMA System. During the experiment, the study found that the FPGA estimation power consumption is reduced when using Recursive IFFT/FFT instead of Complex IFFT/FFT. The result shows a reduction in overall FPGA power by approximately 45%. In addition, reduces the on-chip power and junction temperature and estimates the power consumption during the design cycle of OVLC. The future plane focuses on applying these algorithms to the other modulation using FFT/IIFT for multiplexing the subcarriers.

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