Effects of Thicknesses of Two Different Gate Insulators on the Performance of Pentacene Based Organic Field Effect Transistor

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Abstract

In this paper, a simulation of the electrical performance for Pentacene-based top-contact bottom-gate (TCBG) Organic Field-Effect Transistors (OFET) model with Polymethyl methacrylate (PMMA) and silicon nitride (Si3N4) as gate dielectrics was studied. The effects of gate dielectrics thickness on the device performance were investigated. The thickness of the two gate dielectric materials was in the range of 100-200nm to maintain a large current density and stable performance. MATLAB simulation demonstrated for model simulation results in terms of output and transfer characteristics for drain current and the transconductance. The layer thickness of 200nm may result in gate leakage current points to the requirement of optimizing the thickness of different layers for better performance.

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1. Introduction

The use of organic semiconductor have great interest because of their good facilities, light weight, easy fabrication under ambient condition at low cost [1] . The important of organic semiconductors appear in devices such as transistors [2], solar cell[3], sensor[4], light emitted diode which is serve as active materials. Although, these materials typically exhibit low charge carrier mobility, poor environmental stability and short operational life time comparing with inorganic counterparts[5]. Organic Field effect characteristics have been showed a wide range of organic materials including: polymers, small molecules, oligomers and π-conjugated molecules[6]. Among these materials, Pentacene based OFET show an interested improvement in terms of electrical properties threshold voltage, switching ratio and mobility. The importance of OFET modeling and simulation lies in achieving an optimized design, allowing existing instruments to be used, predicting process control problems, and understanding the mechanism of degradation[7].

Polymer insulators show many advantages compared with inorganic insulators in OFET such as smoother surfaces, no ingrained points sites and processability of solutions. Polymethyl methaacrylate PMMA was chosen in this work since it characteristic as a good insulator. It has low leakage current and used in the lenses of exterior lights of automobile [8-9]. Silicon nitride Si_3N_4 also chosen as inorganic gate dielectric material it has a low density and high temperature strength material, thermodynamically stable and has a high permittivity [10][11].

The effect of two different gate dielectric materials PMMA and Si_3N_4 and the effect of their thicknesses on the electrical characteristics for Pentacene based-OFET were studied in this paper.

2. Device Structure

In this work, a top contact configuration of organic field effect transistor with channel length L=1µm and width W =2.1µm was studied. The gate used in this study was Indium Tin Oxide (ITO) (its work function φ =4.78eV), the used gate dielectric material were Si_3N_4 (dielectric constant ε=7), PMMA (dielectric constant ε=3.5) with thickness 100nm, 150nm and 200nm. Pentacene is the organic semiconductor (300nm thickness) place with gold electrodes for source and drain. These values were chosen depending on several experimental studies. Fig.2 shows schematic structure of OFET.

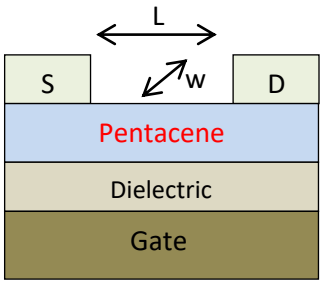

Fig.2: Top-contact configuration of OFET.

3. Characterization using MATLAB Simulation

The electrical characterization of Pentacene-based OFETs was done by using MATLAB simulation. The characterization of organic transistors and materials for the linear and saturation regions of drain current is often analyzed using classical analytically MOS equations. The gradual channel approximation was used to derive the equations, this approximation proposed the field is perpendicular to the current, controlled by the gate bias, is much larger than the electric field between source and drain [12]. At low drain voltage V_d, $|V_d| << |V_g - V_T|$, where V_g is the gate voltage and V_T is the threshold voltage, drain current I_d will increases linearly as V_d increases (linear region) and is determined from the following equation [13-14]:

$$I_d = \frac{WC_i}{L}\mu \times \left[(V_g - V_T) \times V_d - \frac{V_d^2}{2}\right] \qquad (1)$$

For $|V_d| > |V_g - V_T|$, I_d tends to saturate (the saturation regime) due to the "pinch-off" of the accumulation layer and is modeled by the equation

$$I_d = \frac{WC_i}{2L}\mu_{sat.} \times ((V_g - V_T)^2 \quad (2)$$

C_i is capacitance per unit area of the gate insulator, μ is the mobility (5 $Cm^2/V.s$), and V_T is equal to (2.5 V).

4. Results and Discussion

To study the performance of OFET, different gate dielectric thickness of PMMA and Si_3N_4 ranging from 100 – 200nm were studied. Fig. 3 and 4 show I-V characteristics of OFET for both insulator layers (PMMA and Si_3N_4), which indicate an increasing in the current due to thickness increasing, also it can be observed an improvement in the drain current by using PMMA insulator against Si_3N_4 insulator and that is due to the increase of effective capacitance C_i , which is defined as [1]

$$C_i = \varepsilon_\circ \varepsilon / t \quad (3)$$

$\varepsilon_\circ$ is the space permittivity and ε is the material permittivity, the carrier charge density (Q) increasing too

$$Q = C_i(V_g - V_T) \quad (4)$$

In Fig.4 more increasing in the I_d for PMMA/Si3N4, because increasing of the dielectric capacitance C_{total} , which is given by

$$C_{total} = C_{PMMA} + C_{Si3N4} \quad (5)$$

As reducing the insulating thickness, the drain-source current will increase; this can be attributed to the increase of charge carriers with increasing the capacitance for the same gate voltage. Moreover, at lower dielectric thickness, the vertical electric fields will increases this will introduce more holes injected from the source electrode. Therefore; the drain current will increase with reducing dielectric thickness. However, the gate dielectric cannot be too thin because its ability of insulating will maintain and its act as the gate dielectric layer in OFETs.

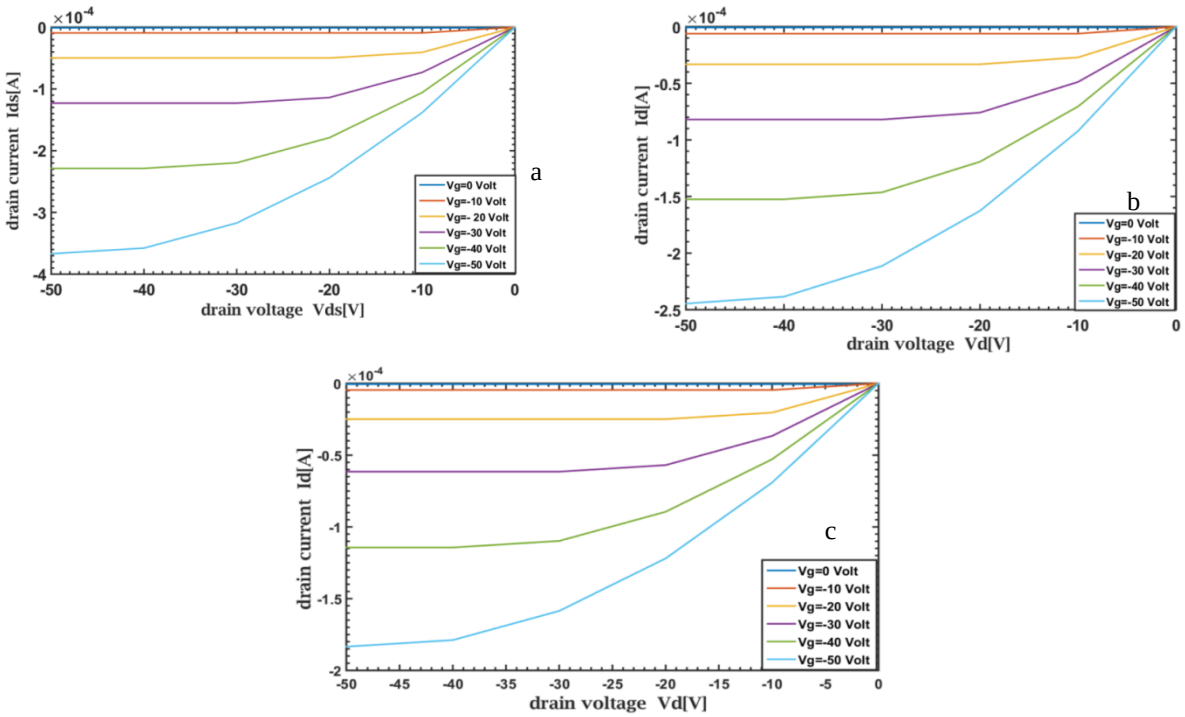

Fig. 3: Output characteristic of gate insulator PMMA at thickness of dielectric a) 100nm b) 150nm and c) 200nm.

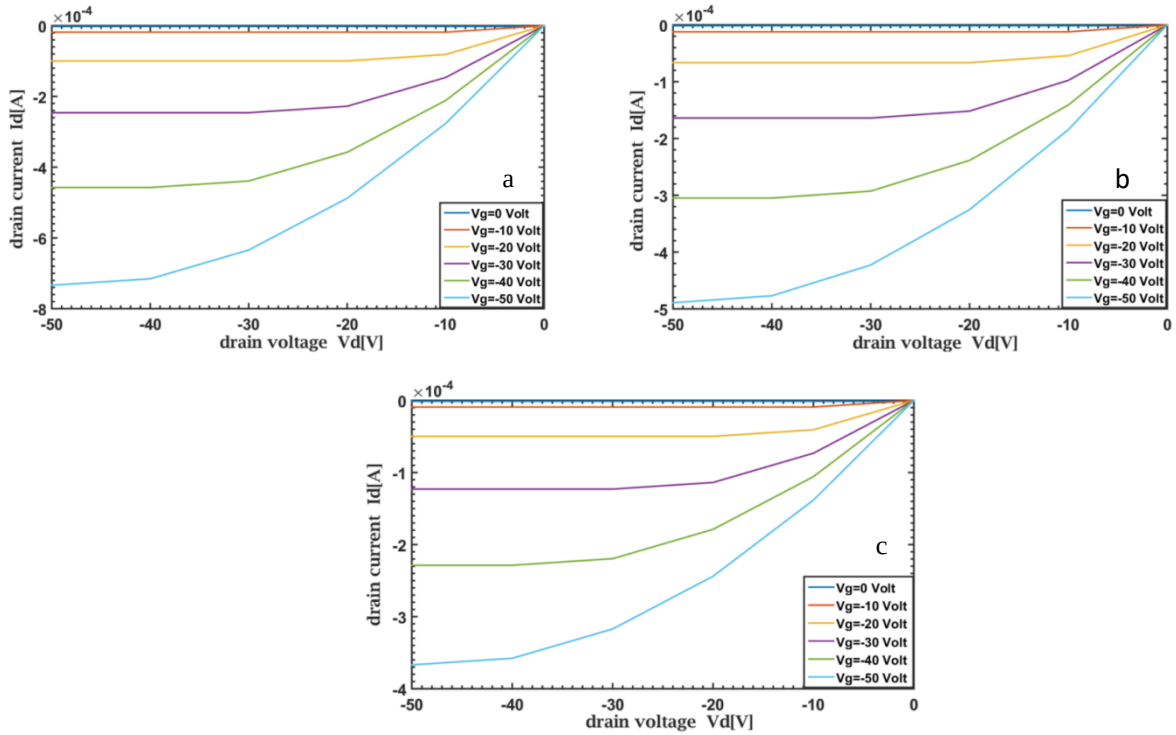

Figure 4: Output characteristic of gate insulator Si_3N_4 at thickness of dielectric a) 100nm b) 150nm and c) 200nm.

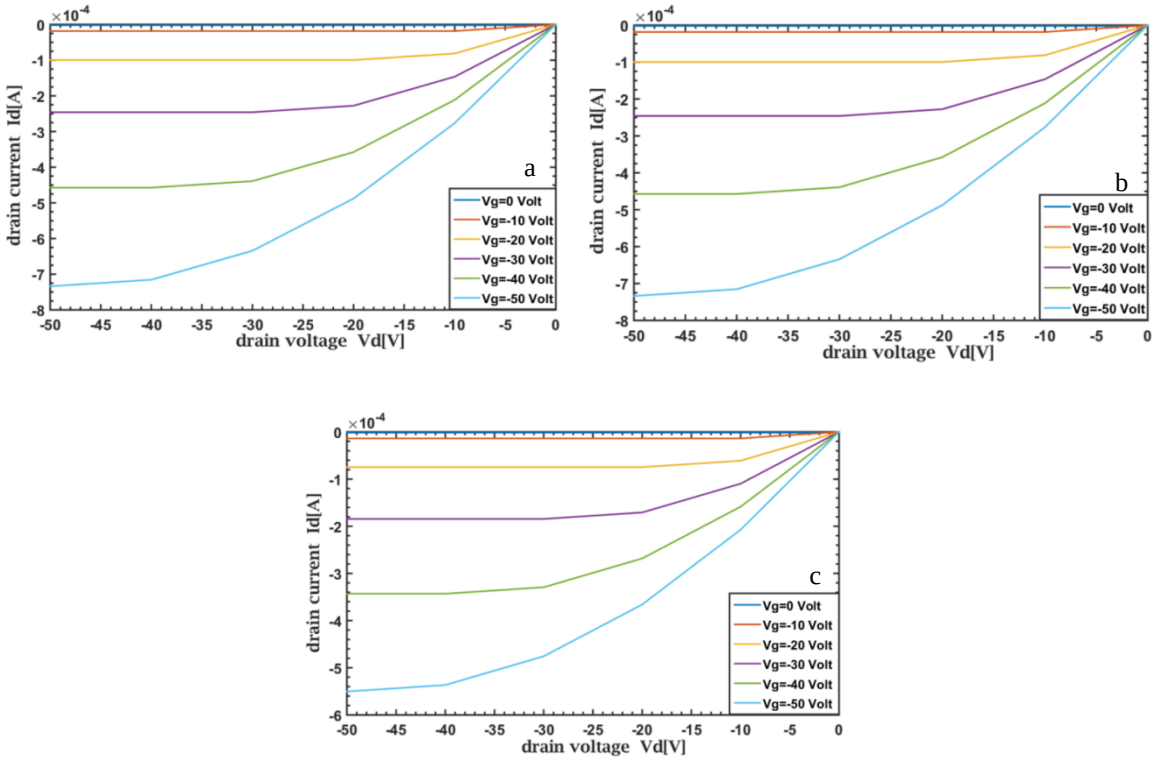

Figure 5: Output characteristic of gate insulator dielectric PMMA/Si_3N_4 at thickness of a)100nm b) 150nm and c) 200nm.

For transfer characteristics shown in figures (6,7 and 8) the same behavior can be estimated where the current is increased by increasing the drain voltage for fixed values of gate voltages. It is clear as the drain bias increased the drain field lowers the source to channel barrier, which increases the charge carrier Q, at the beginning of the channel, and they will cross the barrier. As a result, this will lead to increase the drain current. The best values of the drain current are gotten for dielectric material (PMMA/Si_3N_4) comparing with PMMA and Si_3N_4, Which as illustrated in Fig.8.

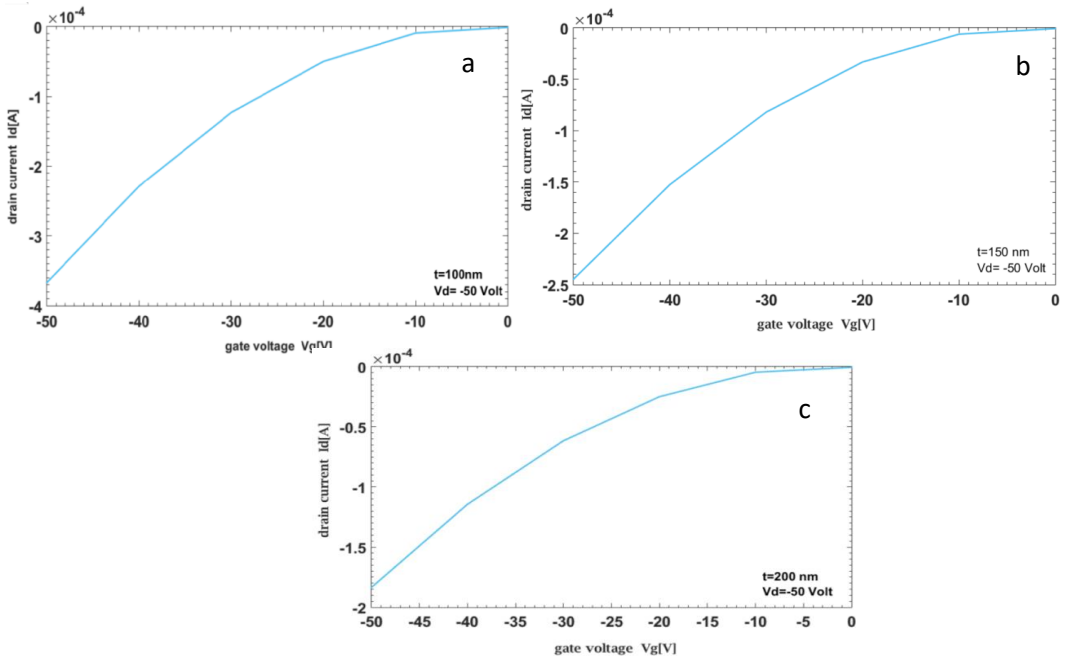

Fig.6: Transfer characteristics at drain voltage -50V of OFETs of gate insulator PMMA at thickness of dielectric a) 100nm b) 150nm and c) 200nm.

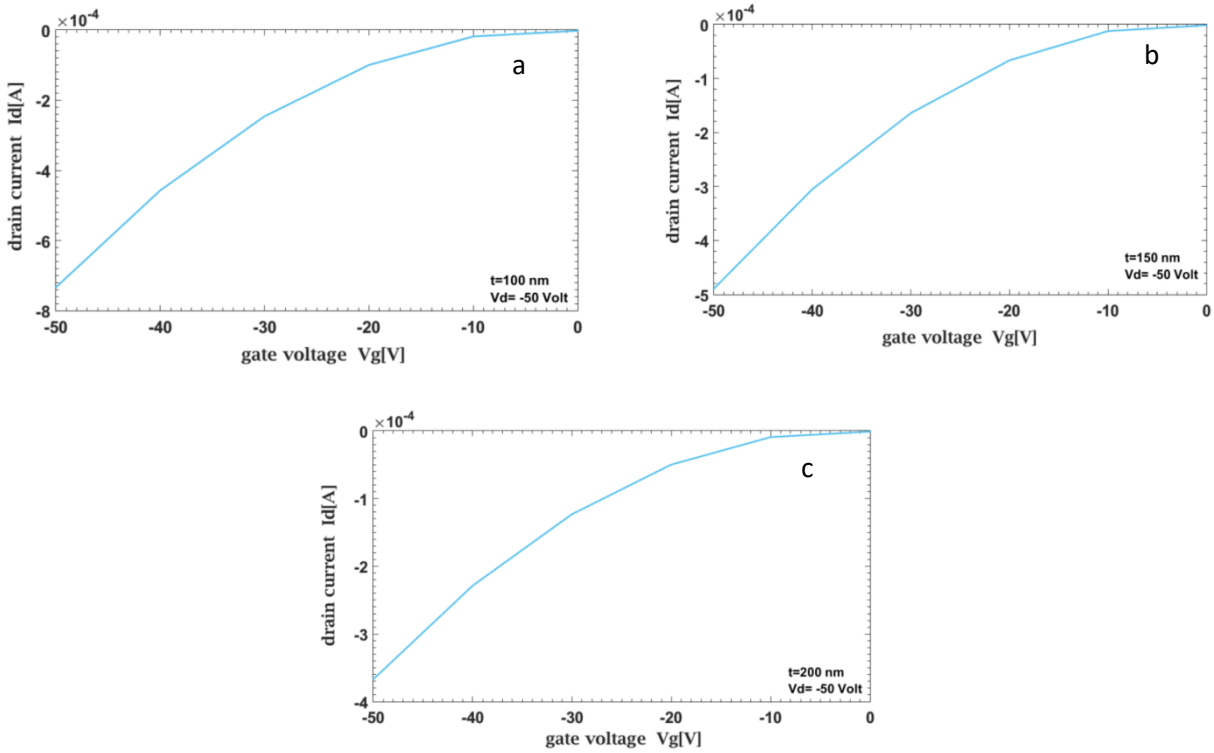

Fig. 7: Transfer characteristics at drain voltage -50V of OFETs of gate insulator Si_3N_4 at thickness of dielectric a)100nm b) 150nm and c) 200nm.

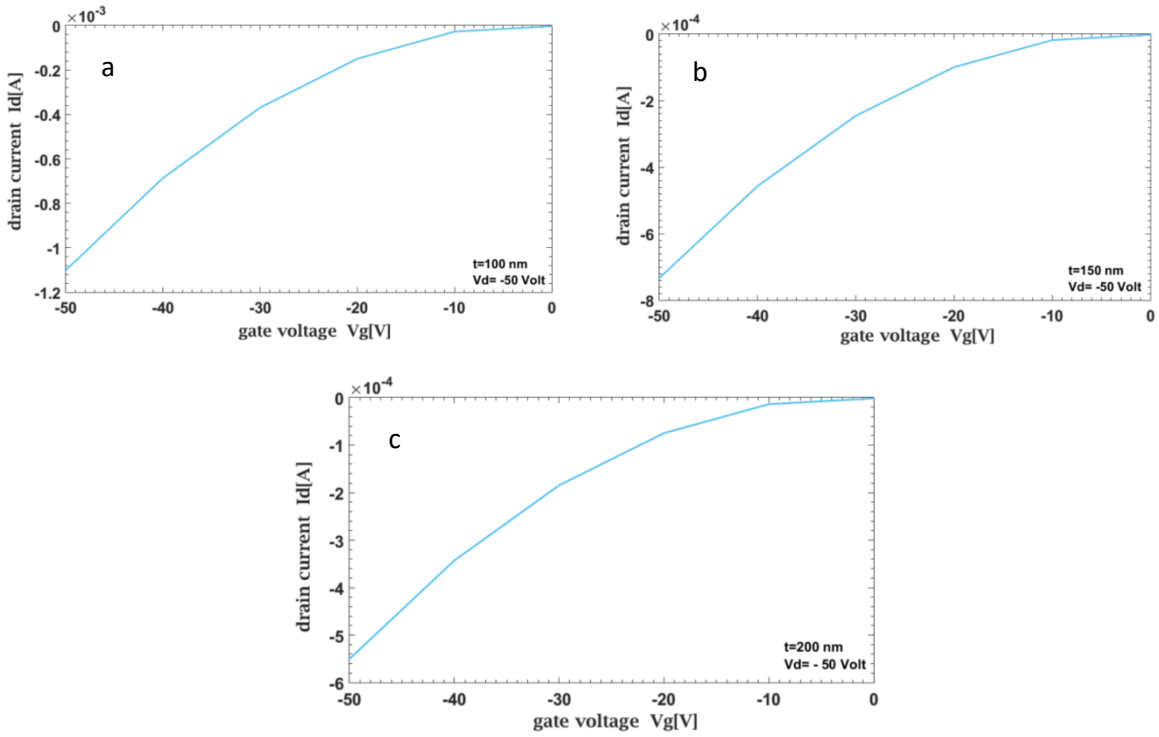

Fig. 8: Transfer characteristics at drain voltage -50V of OFETs of gate insulator PMMA/Si_3N_4 at thickness of dielectric a) 100nm b) 150nm and c) 200nm.

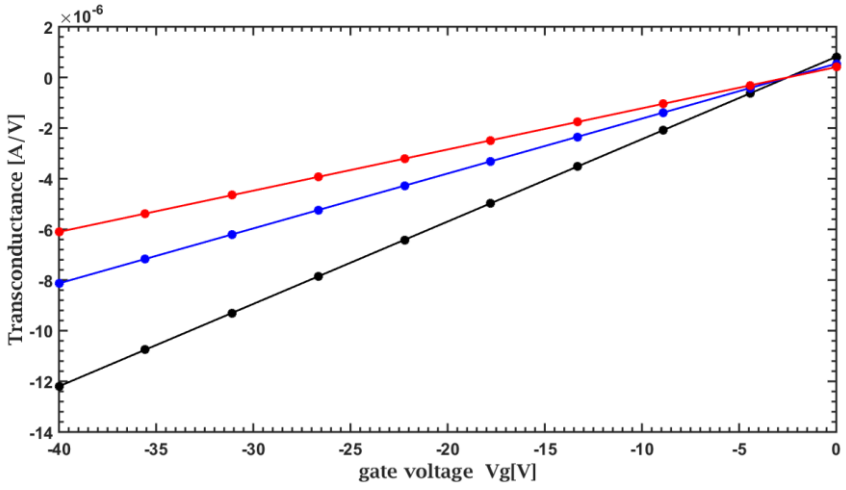

Fig.9: Transconductance at drain voltage -50V of gate insulator PAMM (black line at thickness t=100 nm, blue line at thickness t=150 nm and red line thickness t=200 nm) .

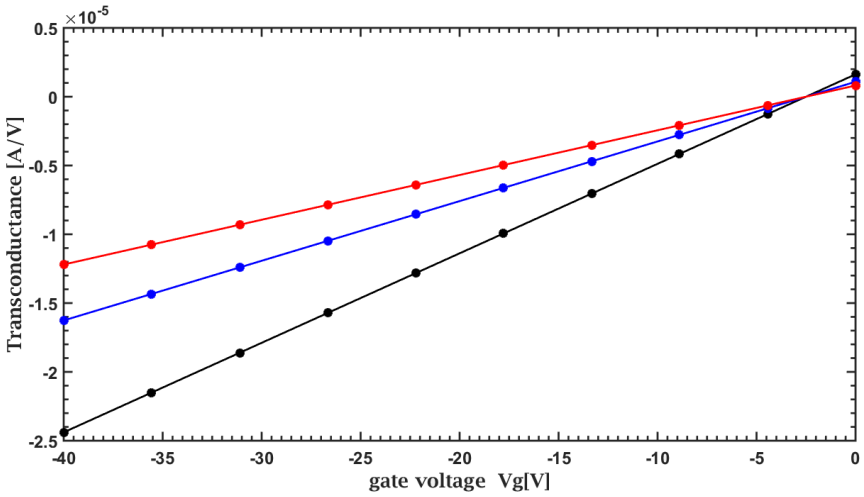

Fig. 10: Transconductance at drain voltage -50V of gate insulator Si_3N_4(black line at thickness t=100 nm, blue line at thickness t=150 nm and red line thickness t=200 nm).

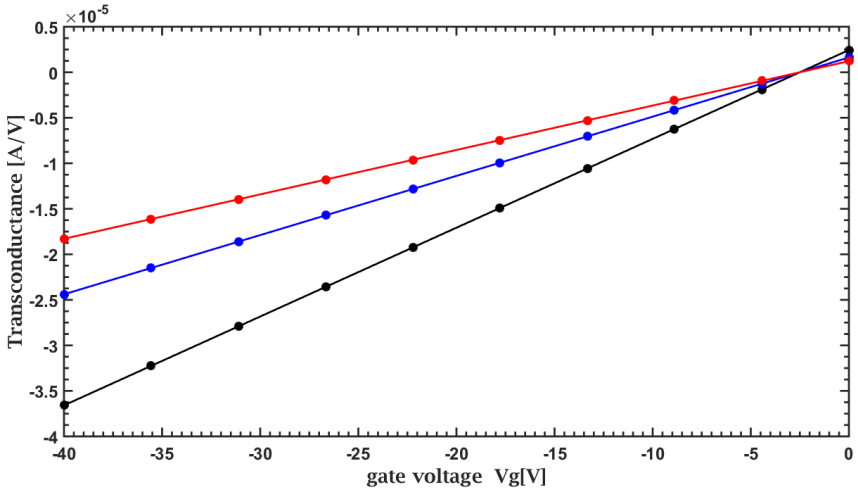

Fig.11: Transconductance at drain voltage -50V of gate insulator Si_3N_4/PAMM(black line at thickness t=100 nm, blue line at thickness t=150 nm and red line thickness t=200 nm) .

5. Conclusions

The results show PMMA, Si_3N_4 can use as gate insulating layers for Pentacene-OFETs. The results indicated the dependence of the device performance on the dielectric constant and its thickness. The results show that electrical characteristics results of the devices increase with increasing dielectric gate. The best performance has been shown in the device with a gate dielectric PMMA with thickness of 100 nm.

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تاثيرات سمك عازلين مختلفين للبوابة على أداء ترانزستور تأثير المجال العضوي القائم على البينتاسين

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المستخلص

تم في هذا البحث دراسة محاكاة للأداء الكهربائي للبوابة السفلية ذات التلامس العلوي لترانزستورات المجال العضوي مع عازلي البوابه بولي مثيل ميثا اكريليت ونيتريد السيليكون. تم دراسة تأثير سماكة عوازل البوابة على أداء الجهاز. كانت سماكة المواد العازلة للبوابتين في حدود 100-200 نانومتر للحفاظ على كثافة تيار كبيرة وأداء مستقر. تم عرض محاكاة MATLAB لنتائج محاكاة النموذج من حيث خصائص الإخراج والتحويل لتيار التصريف والموصلية التحويلية. قد ينتج عن سماكة الطبقة البالغة 200 نانومتر تيار تسرب البوابة والتي تتطلب تحسين سماكة الطبقات المختلفة للحصول على أداء أفضل.